

DATA SHEET



TEA6840H New In Car Entertainment (NICE) car radio

Product specification
Supersedes data of 2001 Mar 08

2003 Feb 04

New In Car Entertainment (NICE) car radio

TEA6840H

| | | | |
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1 FEATURES

- FM mixer for conversion of FM RF from 65 to 108 MHz to IF of 10.7 MHz; the mixer provides inherent image rejection
- FM RF mixer can be set to receive weather band radio up to 162.55 MHz; weather band radio flag output
- AM mixer 1 for conversion of AM RF to AM IF1 of 10.7 MHz
- LC tuner oscillator providing mixer frequencies for FM mixer and AM mixer 1
- AM mixer 2 for conversion of AM IF1 to AM IF2 of 450 kHz
- Crystal oscillator providing mixer frequencies for AM mixer 2 and reference for synthesizer PLL, IF count, timing for Radio Data System (RDS) update and reference frequency for car audio signal processor ICs
- Fast synthesizer PLL tuning system with local control for inaudible RDS updating
- Timing function for RDS update algorithm and control signal output for car audio signal processor ICs (TEA688x, SAA77xx or TEF689x)
- Digital auto alignment circuit for conversion of LC oscillator tuning voltage to controlled alignment voltage of FM antenna tank circuit
- AGC PIN diode drive circuit for FM RF AGC; AGC detection at FM mixer input; the AGC PIN diode drive can be activated by the I²C-bus as a local or distance function; AGC threshold is a programmable and keyed function switchable via the I²C-bus
- FM IF linear amplifiers with high dynamic input range
- FM quadrature demodulator with automatic centre frequency adjustment and Total Harmonic Distortion (THD) compensation
- Level detector for AM and FM with temperature compensated output voltage; starting point and slope of level output is programmable via the I²C-bus
- AM RF PIN diode drive circuit; AGC threshold detection at AM mixer 1 and IF2 AGC input; threshold is programmable via the I²C-bus; AM IF2 AGC and demodulator
- AM AF output switchable to provide AM IF2 for AM stereo decoder
- AM noise blanker with blanking at AM IF2
- Several test modes available for fast IC and system tests.

2 GENERAL DESCRIPTION

The TEA6840H is a single IC with car radio tuner for AM and FM intended for microcontroller tuning with the I²C-bus. It provides the following functions:

- AM double conversion receiver for LW, MW and SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz
- FM single conversion receiver with integrated image rejection for IF = 10.7 MHz capable of selecting US FM, US weather, Europe FM, East Europe FM and Japan FM bands.

3 ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|--|----------|
| | NAME | DESCRIPTION | VERSION |
| TEA6840H | QFP64 | plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm | SOT319-2 |

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4 QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|--|-------|------|--------|------|
| $V_{DDA(n)}$ | analog supply voltage 1, 3, 4, 5 and 6 | | 8 | 8.5 | 9 | V |
| $I_{DDA(tot)}$ | total analog supply current 1, 3, 4, 5 and 6 | FM mode | 45 | 56 | 67 | mA |
| | | AM mode | 39 | 49 | 59 | mA |
| V_{DDA2} | analog supply voltage 2 | | 4.75 | 5 | 5.25 | V |
| I_{DDA2} | analog supply current 2 | FM mode | 6.5 | 8.1 | 9.8 | mA |
| | | AM mode | 4.7 | 5.9 | 7.1 | mA |
| V_{DDD} | digital supply voltage | | 4.75 | 5 | 5.25 | V |
| I_{DDD} | digital supply current | FM mode | 18 | 23 | 28 | mA |
| | | AM mode | 18 | 23 | 28 | mA |
| $f_{AM(ant)}$ | AM input frequency | LW | 0.144 | – | 0.288 | MHz |
| | | MW | 0.522 | – | 1.710 | MHz |
| | | SW | 5.85 | – | 9.99 | MHz |
| $f_{FM(ant)}$ | FM input frequency | | 65 | – | 108 | MHz |
| $f_{FM(WB)(ant)}$ | FM weather band input frequency | | 162.4 | – | 162.55 | MHz |
| T_{amb} | ambient temperature | | –40 | – | +85 | °C |
| AM overall system parameters (1 × SFE10.7MS3; 1 × SFR450H) | | | | | | |
| (S+N)/N | signal plus noise-to-noise ratio | $m = 0.3$ | – | 58 | – | dB |
| THD | total harmonic distortion | $m = 0.8$ | – | 0.3 | – | % |
| | | $m = 0.9$ | – | 0.5 | – | % |
| FM overall system parameters (3 × SFE10.7MS3) | | | | | | |
| (S+N)/N | signal plus noise-to-noise ratio | $\Delta f = 22.5$ kHz; de-emphasis = 50 μ s | – | 65 | – | dB |
| THD | total harmonic distortion | $\Delta f = 75$ kHz | – | 0.6 | 1 | % |

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5 BLOCK DIAGRAM

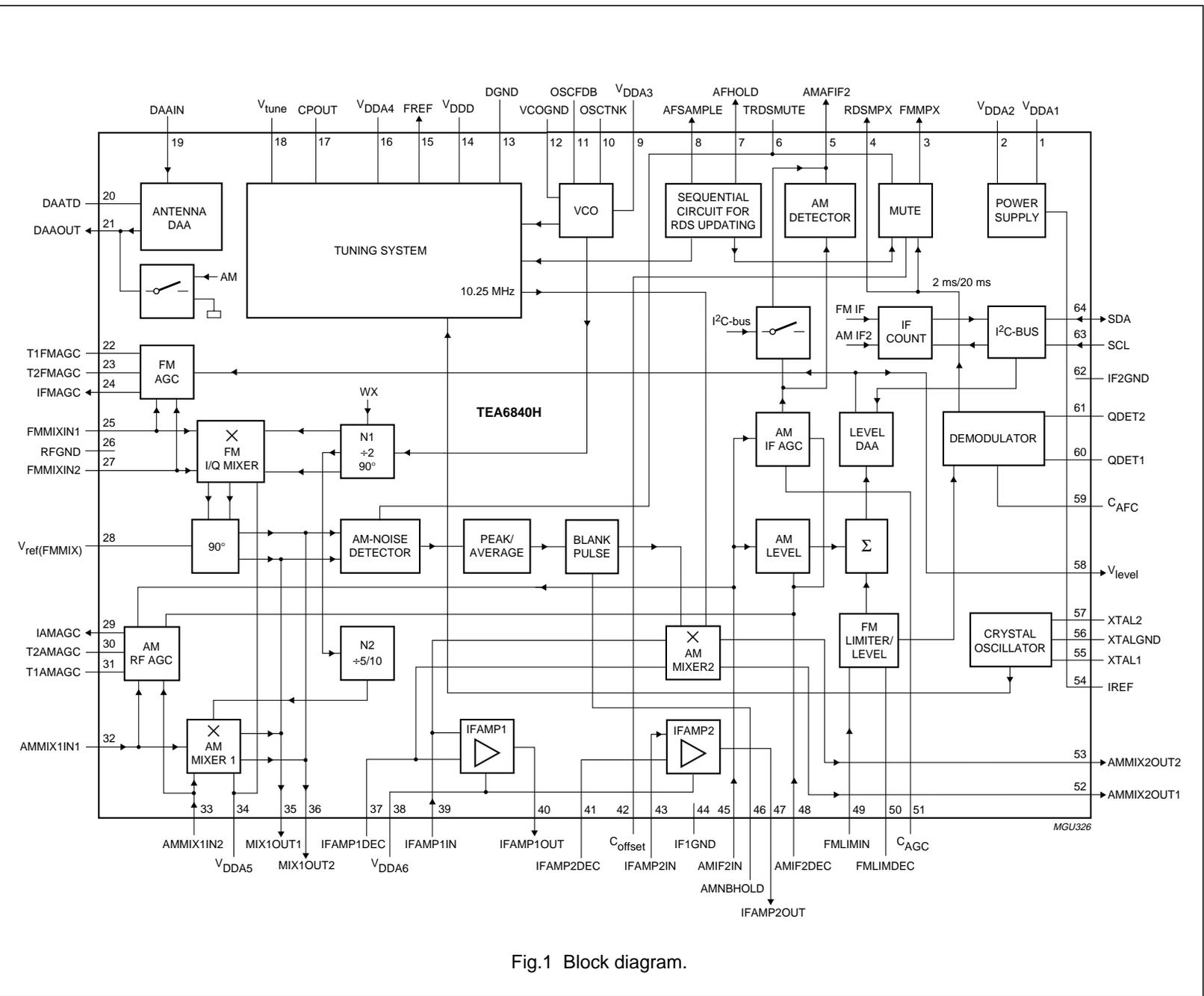


Fig.1 Block diagram.

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6 PINNING

| SYMBOL | PIN | DESCRIPTION |
|-------------------------|-----|--|
| V _{DDA1} | 1 | analog supply voltage 1 (8.5 V) for on-chip power supply |
| V _{DDA2} | 2 | analog supply voltage 2 (5 V) for on-chip power supply |
| FMMPX | 3 | FM demodulator MPX output |
| RDSMPX | 4 | MPX output for RDS decoder and signal processor (not muted) |
| AMAFIF2 | 5 | AM demodulator AF output or IF2 output for AM stereo (multiplexed by I ² C-bus) |
| TRDSMUTE | 6 | time constant for RDS update mute |
| AFHOLD | 7 | AF hold flag output for car audio signal processor IC |
| AFSAMPLE | 8 | AF sample flag output for car audio signal processor IC |
| V _{DDA3} | 9 | analog supply voltage 3 (8.5 V) for VCO |
| OSCTNK | 10 | VCO tank circuit |
| OSCFDB | 11 | VCO feedback |
| VCOGND | 12 | VCO ground |
| DGND | 13 | digital ground |
| V _{DDD} | 14 | digital supply voltage (5 V) |
| FREF | 15 | reference frequency output for signal processor IC |
| V _{DDA4} | 16 | analog supply voltage 4 (8.5 V) for tuning PLL |
| CPOUT | 17 | charge pump output |
| V _{tune} | 18 | tuning voltage |
| DAAIN | 19 | input of digital auto alignment circuit for antenna tank circuit |
| DAATD | 20 | temperature compensation diode for digital auto alignment circuit for antenna tank circuit |
| DAAOUT | 21 | output of digital auto alignment circuit for antenna tank circuit |
| T1FMAGC | 22 | 1st time constant of FM front-end AGC |
| T2FMAGC | 23 | 2nd time constant of FM front-end AGC |
| IFMAGC | 24 | PIN diode drive current output of FM front-end AGC |
| FMMIXIN1 | 25 | FM RF mixer input 1 |
| RFGND | 26 | RF ground |
| FMMIXIN2 | 27 | FM RF mixer input 2 |
| V _{ref(FMMIX)} | 28 | reference voltage for FM I/Q mixer |
| IAMAGC | 29 | PIN diode drive current output of AM front-end AGC |
| T2AMAGC | 30 | 2nd time constant of AM front-end AGC |
| T1AMAGC | 31 | 1st time constant of AM front-end AGC |
| AMMIX1IN1 | 32 | AM mixer 1 input 1 |
| AMMIX1IN2 | 33 | AM mixer 1 input 2 |
| V _{DDA5} | 34 | analog supply voltage 5 (8.5 V) for FM mixer and AM mixer 1 |
| MIX1OUT1 | 35 | FM mixer and AM mixer 1 IF output 1 (10.7 MHz) |
| MIX1OUT2 | 36 | FM mixer and AM mixer 1 IF output 2 (10.7 MHz) |
| IFAMP1DEC | 37 | AM mixer 2 and FM IF amplifier 1 decoupling |
| V _{DDA6} | 38 | analog supply voltage 6 (8.5 V) for IF amplifier 1 and 2 |
| IFAMP1IN | 39 | IF amplifier 1 and AM mixer 2 input (10.7 MHz) |
| IFAMP1OUT | 40 | IF amplifier 1 output (10.7 MHz) |

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| SYMBOL | PIN | DESCRIPTION |
|---------------------|-----|--|
| IFAMP2DEC | 41 | IF amplifier 2 decoupling and AGC capacitor for AM noise blanker |
| C _{offset} | 42 | DC feedback for offset compensation RDS mute |
| IFAMP2IN | 43 | IF amplifier 2 input (10.7 MHz) |
| IF1GND | 44 | AM IF1 ground |
| AMIF2IN | 45 | AM IF2 input (450 kHz) for demodulator AGC and AM level detector |
| AMNBHOLD | 46 | AM noise blanker threshold |
| IFAMP2OUT | 47 | IF amplifier 2 output (10.7 MHz) |
| AMIF2DEC | 48 | decoupling for AM IF2 input |
| FMLIMIN | 49 | FM limiter input (10.7 MHz) |
| FMLIMDEC | 50 | FM limiter decoupling |
| C _{AGC} | 51 | AM IF AGC capacitor |
| AMMIX2OUT1 | 52 | AM mixer 2 output 1 (450 kHz) |
| AMMIX2OUT2 | 53 | AM mixer 2 output 2 (450 kHz) |
| IREF | 54 | reference current for power supply |
| XTAL1 | 55 | crystal oscillator 1 |
| XTALGND | 56 | crystal oscillator ground |
| XTAL2 | 57 | crystal oscillator 2 |
| V _{level} | 58 | level voltage output for AM and FM |
| C _{AFC} | 59 | FM demodulator AFC capacitor |
| QDET1 | 60 | quadrature demodulator tank 1 |
| QDET2 | 61 | quadrature demodulator tank 2 |
| IF2GND | 62 | AM IF2 ground |
| SCL | 63 | I ² C-bus clock line input |
| SDA | 64 | I ² C-bus data line input and output |

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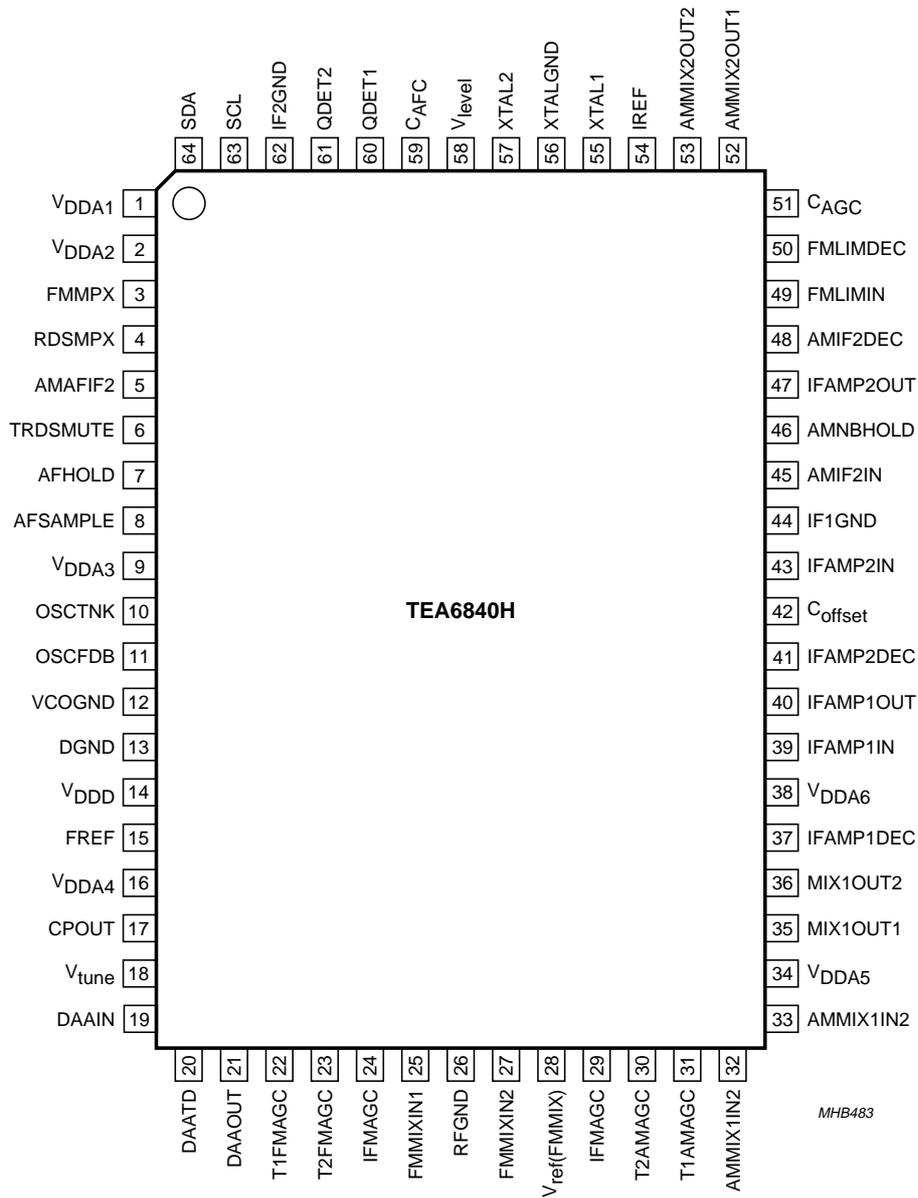


Fig.2 Pin configuration.

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7 FUNCTIONAL DESCRIPTION

7.1 Oscillators

7.1.1 VCO

The L and C tuned VCO provides the local oscillator signal for both FM and AM mixer 1. It has a frequency range of 151.2 to 248.2 MHz.

7.1.2 CRYSTAL OSCILLATOR

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- Local oscillator for AM mixer 2
- Reference frequency for the IF counter
- Timing signal for the RDS update algorithm
- Reference frequency (75.4 kHz) for the TEA688x (car audio signal processor - CASP) or TEF689x (car radio integrated signal processor - CRISP).

7.1.3 PLL

Fast synthesizer PLL tuning system with local control for inaudible RDS updating.

7.2 FM signal channel

7.2.1 DAA

FM RF Digital Auto Alignment (DAA) circuitry for the conversion of the VCO tuning voltage to a controlled alignment voltage for the FM antenna tank circuit.

7.2.2 FM I/Q MIXER

FM quadrature mixer converts FM RF (65 to 162.55 MHz) to IF of 10.7 MHz. The FM mixer provides inherent image rejection and high RF sensitivity.

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands:

- US FM = 87.9 to 107.9 MHz
- US weather FM = 162.4 to 162.55 MHz
- Europe FM = 87.5 to 108 MHz
- Japan FM = 76.0 to 91 MHz
- East Europe FM = 65.8 to 74 MHz.

7.2.3 FM KEYED AGC

FM contains keyed wide-band RF AGC. AGC detection occurs at the FM mixer. The wide-band RF signal switches a narrow band signal (IF) from the FM IF level detector circuitry that controls the FM RF AGC block.

It includes an AGC PIN diode drive circuit for the FM RF AGC. The PIN diode drive can be activated via the I²C-bus as a local or distance function.

The AGC threshold is programmable and the keyed AGC function is switchable via the I²C-bus.

7.2.4 FM IF AMPLIFIERS

The two FM IF amplifiers provide 10 dB and 4 dB amplification with high linearity and dynamic range.

7.2.5 FM DEMODULATOR

The FM quadrature demodulator includes automatic centre frequency adjustment and THD compensation.

7.3 AM signal channel

7.3.1 AM TUNER INCLUDING MIXER 1 AND MIXER 2

The AM tuner is realized in a double conversion technique and is capable of selecting LW, MW and SW bands.

AM mixer 1 converts AM RF to IF1 of 10.7 MHz, while AM mixer 2 converts IF1 of 10.7 MHz to IF2 of 450 kHz:

- LW = 144 to 288 kHz
- MW = 530 to 1710 kHz (US AM band)
- SW = 5.85 to 9.99 MHz (including the 31 m, 41 m and 49 m bands).

7.3.2 AM RF AGC AND IF2 AGC

The AM RF includes a PIN diode drive circuit. The threshold detection points for AM AGC are performed at AM mixer 1 and AM IF2. AGC thresholds are programmable via the I²C-bus.

7.3.3 AM DETECTOR

The AM detector provides AM level information and AM AF or AM IF2.

7.3.4 AM AF OR IF2 SWITCH

The AM output provides either a detected AM AF or the corresponding AM IF2 signal. The IF2 signal can be used for AM stereo decoder processing.

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7.3.5 AM NOISE DETECTOR AND BLANKER

The detection point for the AM noise blanker is the output stage of AM mixer 1, while blanking is realized at the output of the mixer 2.

Trigger sensitivity can be modified by changing the resistor value at pin AMNBHOLD.

7.3.6 FM AND AM LEVEL DETECTOR

FM and AM level detectors provide the temperature compensated output voltage. The starting points and slopes of the level detector outputs are programmable via the I²C-bus.

7.4 Test mode

The test mode of the IC is activated by:

- Sending the test byte (byte 5) to the IC
- Connecting pin FREF through a 100 k Ω resistor to V_{DDA1}
- Applying 50 μ A to pin FREF.

If the test mode is enabled by pin FREF:

- The settling time of the AM IF2 AGC is reduced to less than 100 ms in the nominal application
- The digital-to-analog converters for the antenna DAA and the level DAA can be clocked directly by the SCL line of the I²C-bus
- The output at pin FREF can be selected by the I²C-bus: TEA688x or TEF689x reference frequency, PLL reference frequency or PLL programmable divider output frequency
- The RDS update control circuit can be clocked directly via pin DAATD
- Pin T1AMAGC can be used to enable the load PLL circuit of the RDS update control circuit
- Charge pumps can be set into 3-state mode.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-------------------|--|------------|-------|-------|------|
| V _{DDA1} | analog supply voltage 1 for on-chip power supply | | -0.3 | +10 | V |
| V _{DDA2} | analog supply voltage 2 for on-chip power supply | | -0.3 | +6.5 | V |
| V _{DDA3} | analog supply voltage 3 for VCO | | -0.3 | +10 | V |
| V _{DDA4} | analog supply voltage 4 for tuning PLL | | -0.3 | +10 | V |
| V _{DDA5} | analog supply voltage 5 for FM and AM RF | | -0.3 | +10 | V |
| V _{DDA6} | analog supply voltage 6 for IF amplifier 1 and 2 | | -0.3 | +10 | V |
| V _{DDD} | digital supply voltage | | -0.3 | +6.5 | V |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| T _{amb} | ambient temperature | | -40 | +85 | °C |
| V _{es} | electrostatic handling voltage | note 1 | -200 | +200 | V |
| | | note 2 | -2000 | +2000 | V |

Notes

1. Machine model (R = 0 Ω , C = 200 pF).
2. Human body model (R = 1.5 k Ω , C = 100 pF).

9 THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|----------------------|---|-------------|-------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | 48 | K/W |

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10 DC CHARACTERISTICS

$V_{DDA1} = V_{DDA3} = V_{DDA4} = V_{DDA5} = V_{DDA6} = 8.5\text{ V}$; $V_{DDA2} = 5\text{ V}$; $V_{DDD} = 5\text{ V}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|----------------------------|------|------|------|------------|
| Supply voltage | | | | | | |
| $V_{DDA(n)}$ | analog supply voltage 1, 3, 4, 5 and 6 | | 8 | 8.5 | 9 | V |
| V_{DDA2} | analog supply voltage 2 | | 4.75 | 5 | 5.25 | V |
| V_{DDD} | digital supply voltage | | 4.75 | 5 | 5.25 | V |
| Supply current in FM mode | | | | | | |
| I_{DDD} | digital supply current | | 18 | 23 | 28 | mA |
| I_{DDA1} | analog supply current 1 for on-chip power supply | | – | 15 | – | mA |
| I_{DDA2} | analog supply current 2 for on-chip power supply | | 6.5 | 8.1 | 9.8 | mA |
| I_{DDA3} | analog supply current 3 for VCO | | – | 6.5 | – | mA |
| I_{DDA4} | analog supply current 4 for tuning PLL | test mode; bit TMS3 = 1 | – | 2.9 | – | mA |
| I_{DDA5} | analog supply current 5 for FM RF | | – | 5 | – | mA |
| I_{DDA6} | analog supply current 6 for FM IF amplifier 1 and 2 | | 12 | 14 | 16 | mA |
| $I_{MIX1OUT1}$ | bias current of FM mixer output 1 | | 4.8 | 6 | 7.2 | mA |
| $I_{MIX1OUT2}$ | bias current of FM mixer output 2 | | 4.8 | 6 | 7.2 | mA |
| Supply current in AM mode | | | | | | |
| I_{DDD} | digital supply current | | 18 | 23 | 28 | mA |
| I_{DDA1} | analog supply current 1 for on-chip power supply | | – | 17.5 | – | mA |
| I_{DDA2} | analog supply current 2 for on-chip power supply | | 4.7 | 5.9 | 7.1 | mA |
| I_{DDA3} | analog supply current 3 for VCO | | – | 6.5 | – | mA |
| I_{DDA4} | analog supply current 4 for tuning PLL | test mode; bit TMS3 = 1 | – | 1.6 | – | mA |
| I_{DDA5} | analog supply current 5 for RF | | – | 1.8 | – | mA |
| $I_{MIX1OUT1}$ | bias current of AM mixer 1 output 1 | | 4.8 | 6 | 7.2 | mA |
| $I_{MIX1OUT2}$ | bias current of AM mixer 1 output 2 | | 4.8 | 6 | 7.2 | mA |
| $I_{AMMIX2OUT1}$ | bias current of AM mixer 2 output 1 | | 3.6 | 4.5 | 5.4 | mA |
| $I_{AMMIX2OUT2}$ | bias current of AM mixer 2 output 2 | | 3.6 | 4.5 | 5.4 | mA |
| On-chip power supply reference current generator: pin IREF | | | | | | |
| $V_{O(\text{ref})}$ | output reference voltage | | 4 | 4.25 | 4.5 | V |
| R_o | output resistance | | 8 | 11 | 13 | k Ω |
| $I_{o(\text{max})}$ | maximum output current | | –100 | – | +100 | nA |

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11 AC CHARACTERISTICS

$V_{DDA1} = V_{DDA3} = V_{DDA4} = V_{DDA5} = V_{DDA6} = 8.5 \text{ V}$; $V_{DDA2} = 5 \text{ V}$; $V_{DDD} = 5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; see Figs 9 and 10; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---------------------------------------|--|---------|------|---------|---------------------------------------|
| Voltage controlled oscillator | | | | | | |
| f_{osc} | oscillator frequency | | 151.2 | – | 248.2 | MHz |
| C/N | carrier-to-noise ratio | $f_{\text{osc}} = 200 \text{ MHz}$; $\Delta f = 10 \text{ kHz}$ | – | 101 | – | $\frac{\text{dBc}}{\sqrt{\text{Hz}}}$ |
| RR | ripple rejection | $f_{\text{ripple}} = 100 \text{ Hz}$; $V_{\text{DDA3(ripple)}} = 100 \text{ mV (RMS)}$ | – | 97 | – | dB |
| | | $f_{\text{osc}} = 250 \text{ MHz}$ | – | 99 | – | dB |
| | | $f_{\text{osc}} = 200 \text{ MHz}$ | – | 99 | – | dB |
| FEEDBACK INPUT: PIN OSCFDB | | | | | | |
| $V_{i(\text{bias})}$ | input bias voltage | | 2.2 | 2.8 | 3.4 | V |
| TANK CIRCUIT OUTPUT: PIN OSCTNK | | | | | | |
| V_{O} | DC output voltage | | 5 | 6.1 | 7.2 | V |
| $V_{\text{O(rms)}}$ | AC output voltage (RMS value) | $f_{\text{osc}} = 200 \text{ MHz}$ | – | 1.5 | – | V |
| Crystal oscillator | | | | | | |
| f_{xtal} | crystal frequency | | 20.4996 | 20.5 | 20.5004 | MHz |
| R_{xtal} | crystal motional resistance | start of operating | – | – | 500 | Ω |
| C_{xtal} | crystal shunt capacitance | | – | – | 18 | pF |
| C/N | carrier-to-noise ratio | $f_{\text{xtal}} = 20.5 \text{ MHz (10.25 MHz)}$; $\Delta f = 10 \text{ kHz}$ | – | 112 | – | $\frac{\text{dBc}}{\sqrt{\text{Hz}}}$ |
| CIRCUIT INPUTS: PINS XTAL1, XTAL2 AND XTALGND | | | | | | |
| $V_{\text{xtal(rms)}}$ | crystal voltage (RMS value) | note 1 | – | 350 | – | mV |
| $V_{\text{XTAL1}},$ V_{XTAL2} | DC bias voltage | | 1.7 | 2.1 | 2.5 | V |
| R_i | real part of input impedance | $V_{\text{XTAL1}} - V_{\text{XTAL2}} = 1 \text{ mV}$; note 1 | –500 | – | – | Ω |
| C_i | input capacitance | note 1 | 8 | 10 | 12 | pF |
| I_{XTALGND} | crystal oscillator circuit current | start-up at $V_{\text{XTAL1}} = V_{\text{XTAL2}} = 2.1 \text{ V}$ | – | 9 | – | mA |
| | | operating at $V_{\text{XTAL1}} - V_{\text{XTAL2}} = \pm 400 \text{ mV}$ | – | 1.5 | – | mA |
| Oscillator divider N1 | | | | | | |
| N1 | oscillator divider ratio | FM mode | – | 2 | – | |
| | | standard, Europe and local weather band (WX) | – | 1 | – | |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|--|-----------------------|-----------------------------------|-----------------------|------|
| Oscillator divider N2 | | | | | | |
| N2 | oscillator divider ratio | AM mode LW and MW SW | – – | 10 5 | – – | |
| Synthesizer | | | | | | |
| PROGRAMMABLE DIVIDER | | | | | | |
| N _{prog} | programmable divider ratio | | 512 | – | 32767 | |
| ΔN _{step} | programmable divider step size | | – | 1 | – | |
| REFERENCE FREQUENCY DIVIDER | | | | | | |
| N _{ref} | crystal oscillator divider ratio | f _{xtal} = 20.5 MHz f _{ref} = 100 kHz f _{ref} = 50 kHz f _{ref} = 25 kHz f _{ref} = 20 kHz f _{ref} = 10 kHz | – – – – – | 205 410 820 1025 2050 | – – – – – | |
| CHARGE PUMP: PIN CPOUT | | | | | | |
| I _{sink(cp1)} | low charge pump 1 peak sink current | FM weather band mode; 0.4 V < V _{CPOUT} < 7.6 V | 200 | 300 | 400 | μA |
| I _{source(cp1)} | low charge pump 1 peak source current | FM weather band mode; 0.4 V < V _{CPOUT} < 7.6 V | –400 | –300 | –200 | μA |
| I _{sink(cp1)h} | high charge pump 1 peak sink current | AM stereo mode; N2 = 10 (LW and MW); 0.4 V < V _{CPOUT} < 7.6 V | 0.7 | 1 | 1.3 | mA |
| I _{source(cp1)h} | high charge pump 1 peak source current | AM stereo mode; N2 = 10 (LW and MW); 0.4 V < V _{CPOUT} < 7.6 V | –1.3 | –1 | –0.7 | mA |
| I _{sink(cp2)} | charge pump 2 peak sink current | FM standard mode; 0.3 V < V _{CPOUT} < 7.1 V | 100 | 130 | 160 | μA |
| I _{source(cp2)} | charge pump 2 peak source current | FM standard mode; 0.3 V < V _{CPOUT} < 7.1 V | –160 | –130 | –100 | μA |
| I _{Z(cp1)} , I _{Z(cp2)} | charge pump 1 or 2 current in 3-state | 0 < V _{CPOUT} < 8.5 V | –5 | – | +5 | nA |
| CHARGE PUMP: PIN V _{tune} | | | | | | |
| I _{sink(cp3)} | charge pump 3 peak sink current | FM standard mode; 0.4 V < V _{tune} < 7.6 V | 2.1 | 3 | 3.9 | mA |
| I _{source(cp3)} | charge pump 3 peak source current | FM standard mode; 0.4 V < V _{tune} < 7.6 V | –3.9 | –3 | –2.1 | mA |
| I _{Z(cp3)} | charge pump 3 current in 3-state | 0 < V _{tune} < 8.5 V | –5 | – | +5 | nA |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|--|--------------|-----------|--------------|---------------|
| Antenna Digital Auto Alignment (DAA) | | | | | | |
| DAA INPUT: PIN DAAIN | | | | | | |
| $I_{bias(cp)}$ | charge pump buffer input bias current | FM mode; $0.4\text{ V} < V_{DAAIN} < 8.0\text{ V}$ | -10 | - | +10 | nA |
| | | AM mode; $0\text{ V} < V_{DAAIN} < 8.5\text{ V}$ | -10 | - | +10 | nA |
| $V_{i(cp)}$ | charge pump buffer input voltage | | 0 | - | 8.5 | V |
| DAA OUTPUT: PIN DAAOUT; note 2 | | | | | | |
| $V_{o(AM)}$ | DAA output voltage in AM mode | | - | - | 0.3 | V |
| $V_{o(FM)}$ | DAA output voltage in FM mode | $V_{DAAIN} = 4.0\text{ V};$ $V_{DAAATD} = 0.7\text{ V}$ minimum value | - | - | 0.5 | V |
| | | bits DAA[6:0] set to logic 0 | 1.5 | 1.65 | 1.8 | V |
| | | value: data byte 3 = 10101011 | 3.8 | 4 | 4.2 | V |
| | | maximum value; bits DAA[6:0] set to logic 1 | 8 | - | 8.5 | V |
| | | $V_{DAAIN} = 3.0\text{ V};$ $V_{DAAATD} = 0.7\text{ V};$ bits DAA[6:0] set to logic 1 | 6.2 | 6.5 | 6.8 | V |
| | | $V_{DAAIN} = 2\text{ V}$ data byte 3 = 11010101 | 3 | 3.3 | 3.6 | V |
| | | data byte 3 = 10101010 | 1.8 | 2 | 2.2 | V |
| $V_{o(n)}$ | DAA output noise voltage | FM mode; $V_{DAAIN} = 4\text{ V};$ data byte 3: bit 6 = 1, bits 5 to 0 = 0; B = 300 Hz to 15 kHz | - | 30 | 100 | μV |
| $\Delta V_{o(T)}$ | DAA output voltage variation with temperature | $T_{amb} = -40\text{ to }+85\text{ }^\circ\text{C};$ data byte 3 = 10101011; $V_{DAAATD} = 0.7\text{ V}$ | -8 | - | +8 | mV |
| $\Delta V_{o(step)}$ | DAA step accuracy | FM mode; $V_{DAAOUT} < 8.0\text{ V};$ $n = 0\text{ to }127$ | $0.5V_{LSB}$ | V_{LSB} | $1.5V_{LSB}$ | mV |
| $I_{o(sink)}$ | DAA output sink current | $0.2\text{ V} < V_{DAAOUT} < 8.25\text{ V}$ | 50 | - | - | μA |
| $I_{o(source)}$ | DAA output source current | | - | - | -50 | μA |
| t_{st} | DAA output settling time | $0.2\text{ V} < V_{DAAOUT} < 8.25\text{ V};$ $C_L = 270\text{ pF}$ | - | - | 30 | μs |
| RR | ripple rejection | $f_{ripple} = 100\text{ Hz}; V_{DAA4} = 1\text{ mV}$ | - | 50 | - | dB |
| C_L | DAA output load capacitance | $V_{DAAOUT} < 8.0\text{ V};$ FM mode | - | - | 270 | pF |

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| DAA TEMPERATURE COMPENSATION: PIN DAATD | | | | | | |
| I_{source} | compensation diode source current | $0.2\text{ V} < V_{DAATD} < 1.5\text{ V}$ | -50 | -40 | -30 | μA |
| TC_{source} | temperature coefficient of compensation diode source current | $0.2\text{ V} < V_{DAATD} < 1.5\text{ V};$ $T_{amb} = -40\text{ to }+85\text{ }^{\circ}\text{C}$ | -300 | - | +300 | $\frac{10^{-6}}{\text{K}}$ |
| IF counter (FM IF or AM IF2 counter) | | | | | | |
| N_{IF} | IF counter length for AM and FM | | - | 8 | - | bit |
| $T_{count(IF)}$ | IF counter period | data byte 4: bit 7 = 1 | - | 2 | - | ms |
| | | data byte 4: bit 7 = 0 | - | 20 | - | ms |
| $R_{precount}$ | FM IF counter prescaler ratio | data byte 4: bit 3 = 1 | - | 10 | - | |
| | | data byte 4: bit 3 = 0 | - | 100 | - | |
| Reference frequency for car sound processor IC; note 3 | | | | | | |
| REFERENCE FREQUENCY DIVIDER | | | | | | |
| N_{ref} | crystal oscillator divider ratio | | - | 272 | - | |
| f_{ref} | reference frequency | $f_{xtal} = 20.5\text{ MHz}$ | - | 75.368 | - | kHz |
| VOLTAGE GENERATOR; PIN FREF | | | | | | |
| $V_{o(p-p)}$ | AC output voltage (peak-to-peak value) | | 60 | 100 | 170 | mV |
| V_O | DC output voltage | | 3.2 | 3.4 | 3.9 | V |
| R_o | output resistance | | - | - | 50 | $k\Omega$ |
| $R_{L(min)}$ | minimum load resistance | | 1 | - | - | $M\Omega$ |
| AM signal channel | | | | | | |
| AM RF AGC STAGE INPUTS: PINS AMMIX1IN1 AND AMMIX1IN2 | | | | | | |
| $V_{i(p)}$ | RF input voltage for AGC start level (peak value) | data byte 5: bit 5 = 0, bit 6 = 0 | - | 375 | - | mV |
| | | data byte 5: bit 5 = 1, bit 6 = 0 | - | 500 | - | mV |
| | | data byte 5: bit 5 = 0, bit 6 = 1 | - | 625 | - | mV |
| | | data byte 5: bit 5 = 1, bit 6 = 1 | - | 750 | - | mV |
| AM IF AGC STAGE INPUTS: PINS AMIF2IN AND AMIF2DEC | | | | | | |
| $V_{i(p)}$ | IF2 input voltage (peak value) | AGC start level | 0.5 | 0.85 | 1.0 | V |
| AM RF AGC CURRENT GENERATOR OUTPUT: PIN IAMAGC | | | | | | |
| $I_{sink(max)}$ | maximum AGC sink current | $V_{AMMIX1IN1} > 500\text{ mV}$ (peak value) | - | 15 | - | mA |
| R_o | output resistance | $I_{IAMAGC} = 1\text{ }\mu\text{A}$ | 1 | - | - | $M\Omega$ |
| C_o | output capacitance | | - | 5 | 7 | pF |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|---|------|---------------------|------|------------------------|
| AM RF AGC PEAK DETECTOR: PIN T2AMAGC | | | | | | |
| I_{att} | attack current AGC peak detector | data byte 5: bit 5 = 1, bit 6 = 1; AM mixer 1 input $V_i = 1$ V; $V_{T2AMAGC-GND} = 3$ V; $V_{AMIF2IN-AMIF2DEC} = 0$ V | – | –3.15 | – | mA |
| I_{dec} | decay current AGC peak detector | data byte 5: bit 5 = 1, bit 6 = 1; AM mixer 1 input $V_i = 0$ V; $V_{T2AMAGC-AMMIX1IN2} = 0.25$ V; $V_{T2AMAGC-GND} = 3$ V; $V_{AMIF2IN-AMIF2DEC} = 0$ V | – | 2.6 | – | μ A |
| AM MIXER 1 (IF1 = 10.7 MHz) | | | | | | |
| <i>Mixer inputs: pins AMMIX1IN1 and AMMIX1IN2</i> | | | | | | |
| R_i | input resistance | note 4 | 50 | 70 | 100 | k Ω |
| C_i | input capacitance | note 4 | – | 5 | 7 | pF |
| V_i | DC input voltage | | 2.3 | 2.7 | 3.1 | V |
| $V_{i(max)}$ | maximum voltage on pin AMMIX1IN1 | 1 dB compression point of AM mixer 1 output (peak-to-peak) | 500 | – | – | mV |
| <i>Mixer outputs: pins MIX1OUT1 and MIX1OUT2</i> | | | | | | |
| R_o | output resistance | note 5 | 100 | – | – | k Ω |
| C_o | output capacitance | note 5 | – | 5 | 7 | pF |
| $V_{o(max)(p-p)}$ | maximum output voltage (peak-to-peak value) | | 12 | 15 | – | V |
| I_{bias} | mixer bias current | AM mode | 4.8 | 6 | 7.2 | mA |
| Mixer | | | | | | |
| $g_{m(conv)}$ | conversion transconductance $\frac{I_{MIX1OUT1}}{V_{FMMIXIN1} - FMMIXIN2}$ | | 2.0 | 2.55 | 3.2 | $\frac{mA}{V}$ |
| $g_{m(conv)(T)}$ | conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$ | | – | -9×10^{-4} | – | K $^{-1}$ |
| IP3 | 3rd-order intermodulation | $R_L = 2.8$ k Ω (AC load between output pins) | 135 | 138 | – | dB μ V |
| IP2 | 2nd-order intermodulation | $R_L = 2.8$ k Ω (AC load between output pins) | – | 170 | – | dB μ V |
| $V_{i(n)(eq)}$ | equivalent input noise voltage | band limited noise; $R_{gen} = 750$ Ω ; $R_L = 2.8$ k Ω (AC load between output pins) | – | 5.8 | – | $\frac{nV}{\sqrt{Hz}}$ |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|--|--|------|---------------------|------|--------------------------------------|
| F | noise figure of AM mixer 1 | | – | 4.5 | 7.1 | dB |
| WEATHER BAND FLAG: PIN T1AMAGC | | | | | | |
| $I_{L(max)}$ | maximum load current | | –5 | – | +5 | μA |
| $V_{o(max)}$ | maximum output voltage for FM mode | measured with respect to pin RFGND | 0 | – | 0.5 | V |
| $V_{o(min)}$ | minimum output voltage for WX mode | measured with respect to pin RFGND | 5.1 | 6.0 | 6.9 | V |
| AM MIXER 2 (IF2 = 450 kHz) | | | | | | |
| <i>Mixer inputs: pins IFAMP1IN and IFAMP1DEC</i> | | | | | | |
| R_i | input resistance | note 6 | 270 | 330 | 390 | Ω |
| C_i | input capacitance | note 6 | – | 5 | 7 | pF |
| V_I | DC voltage | | 2.4 | 2.7 | 3 | V |
| $V_{i(max)(p)}$ | maximum input voltage (peak value) | 1 dB compression point of AM mixer 2 output (peak-to-peak) | 1.1 | – | – | V |
| <i>Mixer outputs: pins AMMIX2OUT1 and AMMIX2OUT2</i> | | | | | | |
| R_o | output resistance | note 7 | 100 | – | – | k Ω |
| C_o | output capacitance | note 7 | – | 5 | 7 | pF |
| $V_{o(max)(p-p)}$ | maximum output voltage (peak-to-peak value) | $V_{DDA} = 8.5\text{ V}$ | 12 | 15 | – | V |
| I_{bias} | mixer bias current | AM mode | 3.6 | 4.5 | 5.4 | mA |
| <i>Mixer</i> | | | | | | |
| $g_{m(conv)}$ | conversion transconductance $\frac{I_{AMMIX2OUT1}}{V_{IFAMP1IN}}$ | | 1.3 | 1.6 | 1.9 | $\frac{\text{mA}}{\text{V}}$ |
| $g_{m(conv)(T)}$ | conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$ | | – | -9×10^{-4} | – | K $^{-1}$ |
| IP3 | 3rd-order intermodulation | $R_L = 4\text{ k}\Omega$ (AC load between output pins) | 134 | 137 | – | dB μV |
| IP2 | 2nd-order intermodulation | $R_L = 4\text{ k}\Omega$ (AC load between output pins) | – | 170 | – | dB μV |
| $V_{i(n)(eq)}$ | equivalent input noise voltage | $R_{gen} = 330\ \Omega$; $R_L = 4\text{ k}\Omega$ (AC load between output pins) | – | 15 | 22 | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| F | noise figure of AM mixer 2 | | – | 16 | 19.5 | dB |

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|---|--|---|------------------|--------------------------|----------------------|--------------------------------|
| AM IF2 AGC STAGE: PINS AMIF2IN AND AMIF2DEC; note 8 | | | | | | |
| V_i | input voltage | for $\alpha = -10$ dB audio attenuation AM soft mute on AM soft mute off | – – | 75 6 | 120 10 | μV μV |
| $V_{\text{AGC}(\text{start})}$ | AGC start voltage | input carrier voltage | – | 14 | 30 | μV |
| $V_{\text{AGC}(\text{stop})}$ | AGC stop voltage | maximum input peak voltage | 1 | – | – | V |
| $V_{\text{AGC}(\text{ctrl})}$ | AGC control voltage | $V_i = 1$ mV | 4.1 | 4.3 | 4.7 | V |
| ΔAGC | AGC range | between start and stop of AGC; $m = 0.8$ | – | 89 | – | dB |
| R_i | input resistance | | 1.8 | 2 | 2.2 | $\text{k}\Omega$ |
| C_i | input capacitance | | – | – | 5 | pF |
| AM DETECTOR | | | | | | |
| $V_{\text{sens}(\text{rms})}$ | sensitivity voltage (RMS value) | $m = 0.3$; $f_{\text{mod}} = 400$ Hz; $B_{\text{AF}} = 2.5$ kHz; $R_{\text{gen}} = 2$ $\text{k}\Omega$; note 8 $(\text{S}+\text{N})/\text{N} = 26$ dB $(\text{S}+\text{N})/\text{N} = 46$ dB | – – | 45 600 | 65 900 | μV μV |
| $(\text{S}+\text{N})/\text{N}$ | maximum signal plus noise-to-noise ratio | $m = 0.3$; $f_{\text{mod}} = 400$ Hz; $B_{\text{AF}} = 2.5$ kHz; $R_{\text{gen}} = 2$ $\text{k}\Omega$ | 54 | 60 | – | dB |
| THD | total harmonic distortion | $B_{\text{AF}} = 2.5$ kHz; $C_{\text{AGC}} = 22$ μF ; AM IF2 AGC input $V_i = 100$ μV to 500 mV (RMS) $m = 0.8$; $f_{\text{mod}} = 400$ Hz $m = 0.9$; $f_{\text{mod}} = 400$ Hz $m = 0.8$; $f_{\text{mod}} = 100$ Hz $m = 0.9$; $f_{\text{mod}} = 100$ Hz | – – – – | 0.5 1 1.25 1.75 | 1 2 2.5 3.5 | % % % % |
| RR | ripple rejection | $V_{\text{DDA2}(\text{ripple})} = 100$ mV (RMS); $f_{\text{ripple}} = 100$ Hz | 30 | 40 | – | dB |
| t_{sw} | FM to AM switching time | $C_{\text{AGC}} = 22$ μF | – | 1000 | 1500 | ms |
| t_{settle} | AM AGC settling time | $C_{\text{AGC}} = 22$ μF normal operation test mode | – – | – – | 1800 180 | ms ms |
| <i>Output: pin AMAFIF2</i> | | | | | | |
| $V_{\text{o}(\text{rms})}$ | AM IF2 output voltage (RMS value) | AM stereo; $m = 0$ minimum at $V_i = 14$ μV maximum at $V_i = 5.0$ mV AM mono; $m = 0.3$; $f_{\text{mod}} = 400$ Hz; $V_i = 100$ μV to 500 mV (RMS) | 1.5 130 | 3 180 | 4.5 230 | mV mV mV |
| R_o | output resistance | AM stereo AM mono | – – | – – | 500 500 | Ω Ω |

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|---|---|--|------|------|------|-----------------------------------|
| C_o | output capacitance | AM mono | – | 5 | 7 | pF |
| AM IF2 LEVEL DETECTOR OUTPUT: PIN V_{level} ; see Fig.3 | | | | | | |
| V_{level} | DC output voltage | $V_i = 10 \mu\text{V}$ to 1 V | 0 | – | 7 | V |
| | | $V_i < 1 \mu\text{V}$; standard setting of level DAA and level slope | 0.1 | 0.5 | 0.9 | V |
| | | $V_i = 1.4 \text{ mV}$; standard setting of level DAA | 1.6 | 2.2 | 2.8 | V |
| ΔV_{level} | step size for adjustment of level starting point | standard setting of level slope | 30 | 40 | 50 | mV |
| $V_{level(slope)}$ | slope of level voltage | standard setting of level slope | 650 | 800 | 950 | $\frac{\text{mV}}{20 \text{ dB}}$ |
| ΔV_{step} | step size for adjustment of level slope | $V_i = 1.4 \text{ mV}$ | 45 | 60 | 75 | $\frac{\text{mV}}{20 \text{ dB}}$ |
| B_{level} | bandwidth of level output voltage | | 200 | 300 | – | kHz |
| R_o | output resistance | | – | – | 500 | Ω |
| RR | ripple rejection | $V_{DDA1(ripple)} = 100 \text{ mV (RMS)}$; $f_{ripple} = 100 \text{ Hz}$ | – | 40 | – | dB |
| AM NOISE BLANKER; see Fig.4 | | | | | | |
| <i>Threshold: pin AMNBHOLD</i> | | | | | | |
| V_o | DC output voltage | | 4.3 | 4.6 | 5.1 | V |
| t_{sup} | suppression time | | 6 | 7.5 | 10 | μs |
| $f_{trigger}$ | trigger sensitivity frequency | $V_{pulse} = 200 \text{ mV (peak)}$; $V_{level} < 1.8 \text{ V}$ | – | 1000 | – | Hz |
| | | $V_{pulse} = 200 \text{ mV (peak)}$; $V_{level} > 2.2 \text{ V}$ | – | – | 100 | Hz |
| | | $V_{pulse} = 20 \text{ mV (peak)}$; $V_{level} < 1.8 \text{ V}$ | – | – | 100 | Hz |
| <i>Noise detector output: pin TRDSMUTE</i> | | | | | | |
| $I_{sink(AGC)}$ | AM noise blanker AGC sink current | $V_{TRDSMUTE} = 3 \text{ V}$ | 35 | 50 | 65 | μA |
| V_{AGC} | AM noise blanker AGC voltage | AM mixer 1 input $V_i = 0 \text{ V}$ | 1.9 | 2.2 | 2.5 | V |
| FM signal channel | | | | | | |
| FM RF AGC | | | | | | |
| <i>Inputs: pins FMMIXIN1 and FMMIXIN2; note 9</i> | | | | | | |
| $V_{i(RF)(rms)}$ | RF input voltage for start of wide-band AGC (RMS value) | data byte 5: bit 5 = 0, bit 6 = 0 | – | 4 | – | mV |
| | | data byte 5: bit 5 = 1, bit 6 = 0 | – | 8 | – | mV |
| | | data byte 5: bit 5 = 0, bit 6 = 1 | – | 12 | – | mV |
| | | data byte 5: bit 5 = 1, bit 6 = 1 | – | 16 | – | mV |

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| <i>AGC peak detector output: pin T1FMAGC</i> | | | | | | |
| I_{ch} | charge current | | -350 | -600 | -850 | μA |
| I_{dch} | discharge current | | 15 | 25 | 35 | μA |
| <i>PIN diode drive output: pin IFMAGC</i> | | | | | | |
| I_{drive} | drive current | $V_o = 0.5$ to 4.0 V | 8 | 11.5 | 15 | mA |
| <i>Level voltage output: pin V_{level}</i> | | | | | | |
| V_{th} | threshold voltage for narrow-band AGC | data byte 5: bit 7 = 1; standard setting of level DAA | 500 | 950 | 1400 | mV |
| FM RF MIXER | | | | | | |
| <i>Reference voltage: pin $V_{ref(FMMIX)}$</i> | | | | | | |
| V_{ref} | reference voltage | FM mode | 6.5 | 7.1 | 7.9 | V |
| | | AM mode | 2.7 | 3.1 | 3.4 | V |
| <i>Inputs: pins FMMIXIN1 and FMMIXIN2; note 9</i> | | | | | | |
| $V_{i(RF)(max)}$ | maximum RF input voltage | 1 dB compression point of FM mixer output voltage (peak-to-peak value) | 70 | 100 | - | mV |
| $V_{i(n)(eq)}$ | equivalent input noise voltage | $R_{gen} = 600 \Omega$; $R_L = 2.8 \text{ k}\Omega$ | - | 2.6 | 3.1 | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| R_i | input resistance | | - | 1.4 | - | $\text{k}\Omega$ |
| C_i | input capacitance | | - | 5 | 7 | pF |
| <i>Outputs: pins MIX1OUT1 and MIX1OUT2; note 5</i> | | | | | | |
| R_o | output resistance | | 100 | - | - | $\text{k}\Omega$ |
| C_o | output capacitance | | - | 5 | 7 | pF |
| I_{bias} | mixer bias current | FM mode | 4.8 | 6 | 7.2 | mA |
| $V_{o(max)(p-p)}$ | maximum output voltage (peak-to-peak value) | | 3 | - | - | V |
| FM mixer | | | | | | |
| $g_{m(conv)}$ | conversion transconductance | | 8.5 | 12.5 | 18 | $\frac{\text{mA}}{\text{V}}$ |
| $g_{m(conv)(T)}$ | conversion transconductance variation with temperature | | - | -1×10^{-3} | - | K^{-1} |
| F | noise figure | | - | 3 | 4.6 | dB |
| IP3 | 3rd-order intermodulation | | 116 | 119 | - | $\text{dB}\mu\text{V}$ |
| IRR | image rejection ratio | | 25 | 30 | - | dB |
| IF AMPLIFIER 1 | | | | | | |
| G | gain | $R_L = 330 \Omega$; $V_i = 1 \text{ mV}$; note 10 | 8.5 | 10.5 | 12.5 | dB |
| F | noise figure | | - | 9.5 | 13 | dB |
| IP3 | 3rd-order intermodulation | | 120 | 123 | - | $\text{dB}\mu\text{V}$ |

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|--|-------------------------------------|--|------|------|------|------------------------|
| <i>Inputs: pins IFAMP1IN and IFAMP1DEC; note 10</i> | | | | | | |
| $V_{i(max)(p)}$ | maximum input voltage (peak value) | 1 dB compression point of IF amplifier 1 output voltage (peak value) | 300 | – | – | mV |
| $V_{i(n)(eq)}$ | equivalent input noise voltage | $R_{gen} = 330 \Omega$; $R_L = 330 \Omega$ | – | 7 | 10 | $\frac{nV}{\sqrt{Hz}}$ |
| R_i | input resistance | | 270 | 330 | 390 | Ω |
| C_i | input capacitance | | – | 5 | 7 | pF |
| <i>Output: pin IFAMP1OUT</i> | | | | | | |
| $V_{o(max)(p)}$ | maximum output voltage (peak value) | | 1.2 | 1.5 | – | V |
| R_o | output resistance | | 270 | 330 | 390 | Ω |
| C_o | output capacitance | | – | 5 | 7 | pF |
| IF AMPLIFIER 2 | | | | | | |
| G | gain | $R_L = 330 \Omega$; $V_i = 1 \text{ mV}$; note 11 | 3 | 4.5 | 6 | dB |
| F | noise figure | | – | 12 | 15 | dB |
| IP3 | 3rd-order intermodulation | | 129 | 132 | – | dB μ V |
| <i>Inputs: pins IFAMP2IN and IFAMP2DEC; note 11</i> | | | | | | |
| $V_{i(max)(p)}$ | maximum input voltage (peak value) | 1 dB compression point of IF amplifier 2 output voltage (peak value) | 600 | – | – | mV |
| $V_{i(n)(eq)}$ | equivalent input noise voltage | $R_{gen} = 330 \Omega$; $R_L = 330 \Omega$ | – | 9 | 12 | $\frac{nV}{\sqrt{Hz}}$ |
| R_i | input resistance | | 270 | 330 | 390 | Ω |
| C_i | input capacitance | | – | 5 | 7 | pF |
| <i>Output: pin IFAMP2OUT</i> | | | | | | |
| $V_{o(max)(p)}$ | maximum output voltage (peak value) | | 1.2 | 1.5 | – | V |
| R_o | output resistance | | 270 | 330 | 390 | Ω |
| C_o | output capacitance | | – | 5 | 7 | pF |
| FM demodulator and level detector; see Figs 5 and 6 | | | | | | |
| FM LIMITER | | | | | | |
| <i>Inputs: pins FMLIMIN and FMLIMDEC; note 12</i> | | | | | | |
| G | gain | $R_{gen} = 50 \Omega$ | 74 | 80 | – | dB |
| R_i | input resistance | | 270 | 330 | 390 | k Ω |
| C_i | input capacitance | | – | 5 | 7 | pF |
| <i>Outputs: pins QDET1 and QDET2</i> | | | | | | |
| $V_{o(p-p)}$ | output voltage (peak-to-peak value) | measured between output pins | 500 | 700 | – | mV |

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|--|--|--|------|------|------|------------|
| FM DEMODULATOR | | | | | | |
| R_L | load resistance | | 20 | – | – | k Ω |
| C_L | load capacitance | | – | – | 50 | pF |
| <i>FM limiter inputs: pins FMLIMIN and FMLIMDEC; note 12</i> | | | | | | |
| $V_{\text{start(lim)(rms)}}$ | start of limiting of MPX output voltage (RMS value) | $\alpha_{AF} = -3$ dB | – | 10 | 15 | μ V |
| $V_{\text{o(sens)(rms)}}$ | sensitivity for MPX output voltage (RMS value) | $\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 μ s | – | 10 | 15 | μ V |
| | | (S+N)/N = 26 dB | – | 50 | 75 | μ V |
| <i>RDS MPX output: pin RDSMPX</i> | | | | | | |
| $V_{\text{o(rms)}}$ | RDS MPX output voltage (RMS value) | $\Delta f = 22.5$ kHz; $f_{\text{mod}} = 57$ kHz; $V_i = 20$ μ V to 1 V; note 12 | 180 | 230 | 280 | mV |
| $I_{\text{o(max)}}$ | maximum RDS MPX output current | | – | – | 100 | μ A |
| R_o | output resistance | | – | – | 500 | Ω |
| B | bandwidth RDS MPX output | $C_L = 0$; $R_L > 20$ k Ω | 200 | 300 | – | kHz |
| PSRR | power supply ripple rejection | $f_{\text{ripple}} = 100$ Hz to 20 kHz | – | 40 | – | dB |
| <i>FM MPX output: pin FMMPX; note 12</i> | | | | | | |
| $V_{\text{o(rms)}}$ | MPX output voltage (RMS value) | $\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 μ s; $V_i = 20$ μ V to 1 V | 180 | 230 | 280 | mV |
| α_{AM} | AM suppression of MPX output | $\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; m = 0.3; de-emphasis = 75 μ s $V_i = 500$ μ V to 300 mV | 50 | 60 | – | dB |
| | | $V_i = 20$ to 500 μ V | – | 40 | – | dB |
| | | $V_i = 300$ mV to 1 V | – | 40 | – | dB |
| $I_{\text{o(max)}}$ | maximum MPX output current | | – | – | 100 | μ A |
| (S+N)/N | maximum signal plus noise-to-noise ratio of MPX output voltage | $\Delta f = 22.5$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 μ s; $V_i = 10$ mV | 67 | 70 | – | dB |
| THD | total harmonic distortion of MPX output voltage | $\Delta f = 75$ kHz; $f_{\text{mod}} = 1$ kHz; de-emphasis = 75 μ s; $V_i = 200$ μ V to 800 mV | – | 0.35 | 0.7 | % |
| B | bandwidth MPX output | $C_L = 0$; $R_L > 20$ k Ω | 200 | – | – | kHz |
| PSRR | power supply ripple rejection | $f_{\text{ripple}} = 100$ Hz to 20 kHz | – | 40 | – | dB |
| $R_{L(\text{min})}$ | minimum load resistance | | 20 | – | – | k Ω |

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| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|--|------|-------|------|-----------------------------------|
| $R_{o(max)}$ | maximum output resistance | | – | – | 500 | Ω |
| $C_{L(max)}$ | maximum load capacitance | | – | – | 50 | pF |
| MPX MUTE | | | | | | |
| α_{mute} | muting depth | during RDS update | 60 | 80 | – | dB |
| t_{att} | attack time MPX mute | $C_{TRDSMUTE} = 10 \text{ nF}$ | 0.75 | 1 | 1.25 | ms |
| t_{decay} | decay time MPX mute | $C_{TRDSMUTE} = 10 \text{ nF}$ | 0.75 | 1 | 1.25 | ms |
| <i>RDS update: pin TRDSMUTE</i> | | | | | | |
| I_{dch} | discharge current | $V_o = 3 \text{ V}$; audio output muted | 24 | 32 | 38 | μA |
| I_{ch} | charge current | $V_o = 3 \text{ V}$; audio output not muted | –38 | –32 | –24 | μA |
| DEMODULATOR AFC | | | | | | |
| G_{AFC} | AFC gain | $\Delta f = 100 \text{ kHz}$ | 28 | 32 | – | dB |
| <i>RDS MPX output: pin RDSMPX; note 12</i> | | | | | | |
| $V_{offset(DC)}$ | residual DC offset voltage | $L_{demod} = \text{typical value}$ | – | 0.1 | 1 | V |
| | | $V_i = 10 \text{ to } 80 \mu\text{V}$ | – | 10 | 30 | mV |
| | | $V_i = 80 \mu\text{V to } 800 \text{ mV}$ | – | 0.240 | 1 | V |
| | | $L_{demod} = \pm 6\%$ | – | 25 | 500 | mV |
| FM IF LEVEL DETECTOR OUTPUT: PIN V_{level}; note 12 | | | | | | |
| V_{level} | DC output voltage | $V_i = 10 \mu\text{V to } 1 \text{ V}$ | 0 | – | 7 | V |
| | | $V_i < 1 \mu\text{V}$; standard setting of level DAA | 0.1 | 0.35 | 0.9 | V |
| | | $V_i = 1 \text{ mV}$; standard setting of level DAA | 1 | 1.5 | 2.1 | V |
| ΔV_{level} | level starting point for adjustment of step size | standard setting of level slope | 30 | 40 | 50 | mV |
| $V_{level(slope)}$ | slope of level voltage | standard setting of level slope | 650 | 800 | 950 | $\frac{\text{mV}}{20 \text{ dB}}$ |
| ΔV_{step} | level slope adjustment of step size | $V_i = 1 \text{ mV}$ | 45 | 50 | 75 | $\frac{\text{mV}}{20 \text{ dB}}$ |
| B_{level} | bandwidth of level output voltage | $V_i = 10 \text{ mV}$; $f_{mod} = 22.5 \text{ kHz}$; standard setting of level DAA | 200 | 300 | – | kHz |
| R_o | output resistance | | – | – | 500 | Ω |
| RR | ripple rejection | $V_{DDA1(ripple)} = 100 \text{ mV (RMS)}$; $f_{ripple} = 100 \text{ Hz}$ | – | 40 | – | dB |

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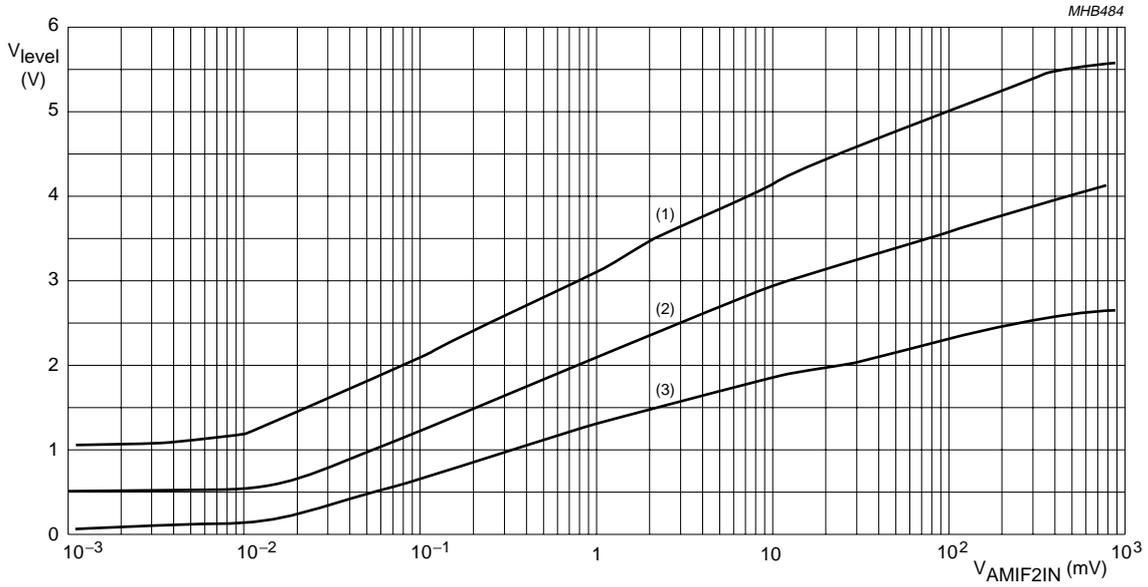
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--|---|---|------|------|------|------|
| RDS update | | | | | | |
| <i>Output: pin AFHOLD</i> | | | | | | |
| $I_{\text{sink(max)}}$ | maximum sink current | after first bus transmission with AF = 1 (start of RDS update); $V_o = 0.5 \text{ V}$ | 1.0 | 1.2 | 1.4 | mA |
| <i>Output: pin AFSAMPLE</i> | | | | | | |
| $I_{\text{sink(max)}}$ | maximum sink current | no RDS update in progress; $V_o = 0.5 \text{ V}$ | 1.0 | 1.2 | 1.4 | mA |
| Test mode; note 3 | | | | | | |
| <i>Temperature compensation diode: pin DAATD</i> | | | | | | |
| $V_{i(\text{ext})}$ | external input voltage to clock state machine | $V_{\text{DAATD(L)}} = 2.5 \text{ V};$ $V_{\text{DAATD(H)}} = 3.5 \text{ V}$ | 2.5 | – | 3.5 | V |
| <i>Clock input: pin SCL</i> | | | | | | |
| $V_{i(\text{ext})}$ | external input voltage to clock DAA | $V_{\text{SCL(L)}} = 0 \text{ V}; V_{\text{SCL(H)}} = 5 \text{ V}$ | 0 | – | 5 | V |
| <i>Time constant output: pin T1AMAGC</i> | | | | | | |
| V_{pulse} | enabling voltage of load PLL signal | pin FREF in test mode | 5.1 | 6 | 6.9 | V |

Notes

1. Measured between pins XTAL1 and XTAL2.
2. DAA conversion gain formula: $V_{\text{DAAOUT}} = \left[2 \times \left(0.75 \times \frac{n}{128} + 0.25 \right) \times (V_{\text{DAAIN}} + V_{\text{DAATD}}) \right] - V_{\text{DAATD}}$
where $n = 0$ to 127.
3. Reference frequency pin FREF:
 - a) $R_{\text{ext}} = 68 \text{ k}\Omega$ connected to ground activates the 2nd I²C-bus address
 - b) $R_{\text{ext}} = 100 \text{ k}\Omega$ connected to V_{DDA1} sets the IC into test mode.
4. Input parameters of AM mixer 1 measured between pins AMMIX1IN1 and AMMIX1IN2.
5. Output parameters of FM mixer and AM mixer 1 measured between pins MIX1OUT1 and MIX1OUT2.
6. Input parameters of AM mixer 2 measured between pins IFAMP1IN and IFAMP1DEC.
7. Output parameters of AM mixer 2 measured between pins AMMIX2OUT1 and AMMIX2OUT2.
8. Input parameters of AM IF2 measured between pins AMIF2IN and AMIF2DEC.
9. Input parameters of FM mixer measured between pins FMMIXIN1 and FMMIXIN2.
10. Input parameters of IF amplifier 1 measured between pins IFAMP1IN and IFAMP1DEC.
11. Input parameters of IF amplifier 2 measured between pins IFAMP2IN and IFAMP2DEC.
12. Input parameters of FM limiter measured between pins FMLIMIN and FMLIMDEC.

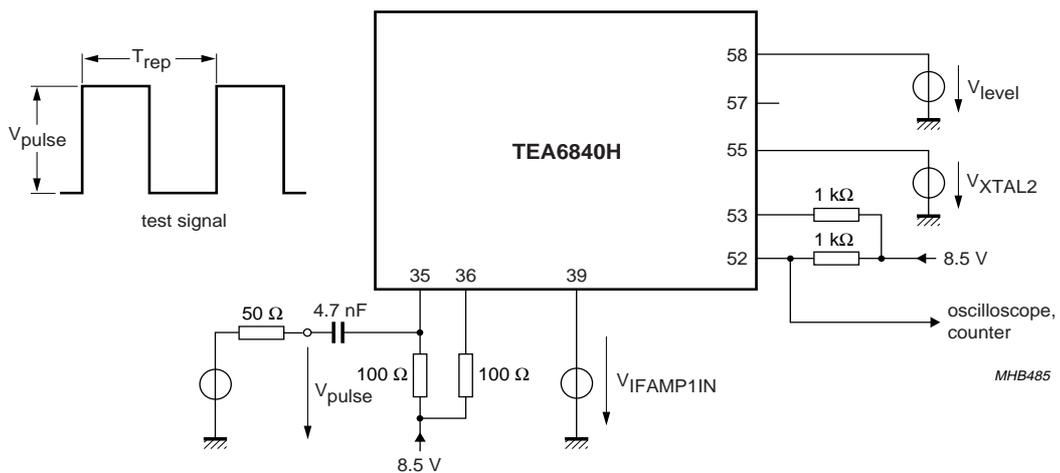
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- (1) Level DAA setting byte 6 = FFH.
- (2) Level DAA setting byte 6 = 84H (standard setting).
- (3) Level DAA setting byte 6 = 00H.

Fig.3 AM level output voltage (DAA) as a function of AM level circuit input voltage.



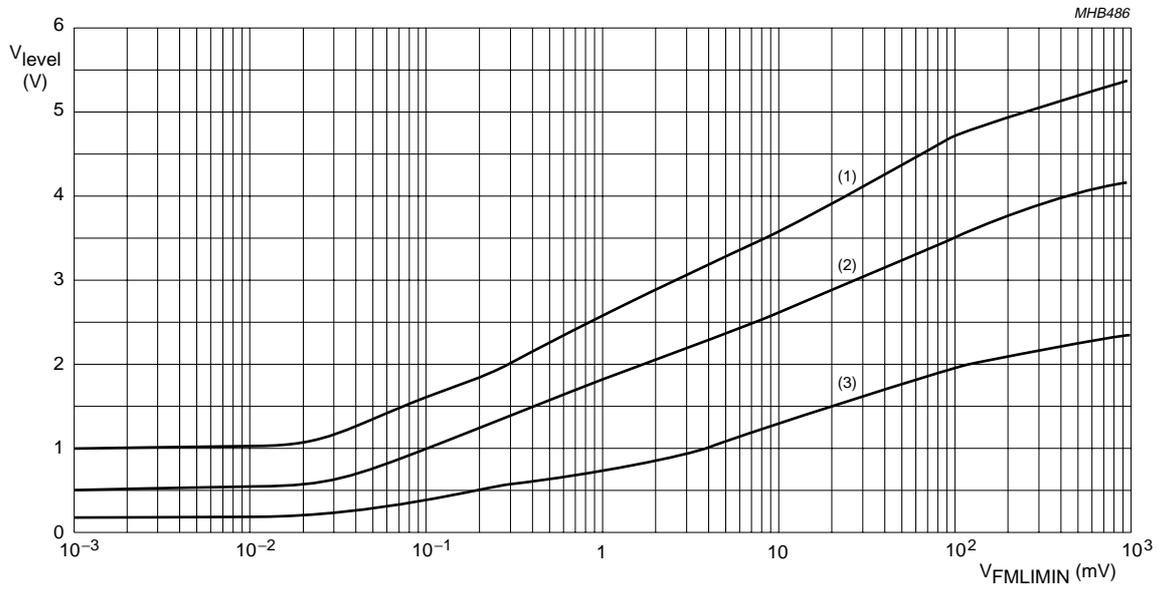
Test signal: $T_{rep} = 2 \text{ ms}$, $t_r < 50 \text{ ns}$, $t_f < 50 \text{ ns}$, and duty factor 50%.

$V_{IFAMP1IN} = 4 \text{ V}$.
 $V_{XTAL2} = 3 \text{ V}$.

Fig.4 Test circuit for AM noise blanker.

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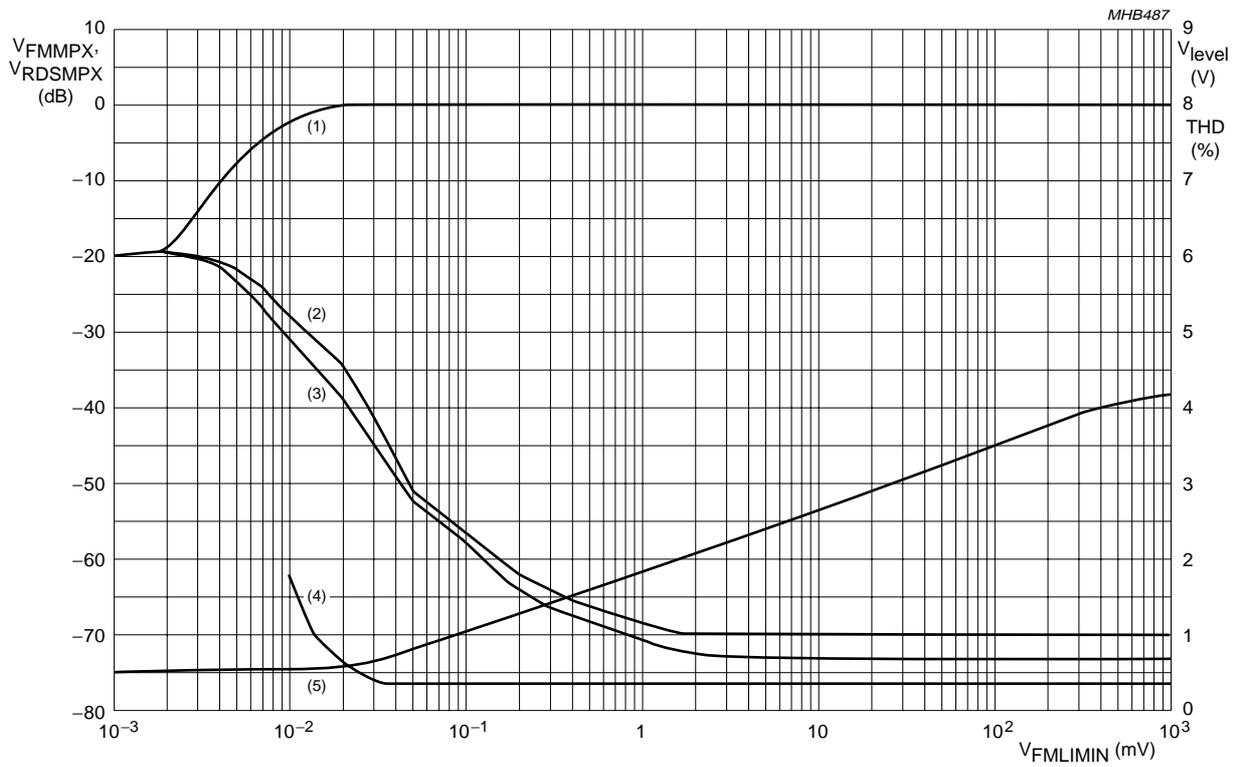


- (1) Level DAA setting byte 6 = FFH.
- (2) Level DAA setting byte 6 = 84H (standard setting).
- (3) Level DAA setting byte 6 = 00H.

Fig.5 FM level output voltage (DAA) as a function of FM limiter and level circuit input voltage.

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- (1) Output voltage for FMMPX and RDSMPX: $f_{IF} = 10.7$ MHz; $\Delta f = 22.5$ kHz; $f_{mod} = 1$ kHz.
- (2) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 μ s for FMMPX.
- (3) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 μ s for RDSMPX.
- (4) THD for FMMPX and RDSMPX.
- (5) Level for standard setting of level DAA, byte 6 = 84H.

Fig.6 (S+N)/N, THD and level output voltage for FM mode as a function of FM demodulator input voltage.

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12 I²C-BUS PROTOCOL

12.1 I²C-bus specification

The standard I²C-bus specification is expanded by the following definitions.

IC addresses:

- 1st IC address C2: 1100001
- 2nd IC address C0: 1100000.

Structure of the I²C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

Exception to the standard I²C-bus specification:

- The data hold time $t_{HD;DAT}$ must be at least 1 μ s.

12.1.1 TEST MODE

Connecting pin FREF to V_{DDA1} via a 100 k Ω resistor or feeding 50 μ A into that pin switches the IC into the test mode.

During test mode the digital-to-analog converters of the level and antenna DAA functions can be sequenced by the I²C-bus SCL line.

During test mode either the TEA688x or TEF689x reference frequency, the PLL reference frequency divider or the programmable divider output can be switched to pin FREF.

12.1.2 DATA TRANSFER

Data sequence: address, byte 1, byte 2, byte 3, byte 4, byte 5, and byte 6.

The data transfer has to be in this order. The LSB = 0 indicates a WRITE operation to the TEA6840H.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available.

In byte 5, 4 bits are reserved for test mode purposes. Those can only be used when the test mode is activated by the select pin FREF.

12.1.3 I²C-BUS PULL-UP RESISTORS

When the IC is used together with the TEA688x or TEF689x and both SCL and SDA lines are connected via the I²C-bus to the TEA688x or TEF689x, the pull-up resistors of the tuner IC should be connected to the digital supply voltage of the TEA688x or TEF689x. Otherwise an I²C-bus pull-down can occur switching off the tuner IC supply when the I²C-bus buffer interface of the TEA688x or TEF689x is enabled for data transfer to the tuner IC.

12.1.4 FREQUENCY SETTING

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting bit MUTE = 1. To select an FM frequency, two I²C-bus transmissions are necessary:

- First: bit MUTE = 1
- Second: bit MUTE = 0.

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12.2 I²C-bus protocol

12.2.1 DATA TRANSFER MODE AND IC ADDRESS

Table 1 Write mode

| | | | | | |
|------------------|-----------------|------------------|--------------|------------------|------------------|
| S ⁽¹⁾ | address (write) | A ⁽²⁾ | data byte(s) | A ⁽²⁾ | P ⁽³⁾ |
|------------------|-----------------|------------------|--------------|------------------|------------------|

Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 2 Read mode

| | | | |
|------------------|----------------|------------------|-------------|
| S ⁽¹⁾ | address (read) | A ⁽²⁾ | data byte 1 |
|------------------|----------------|------------------|-------------|

Notes

1. S = START condition.
2. A = acknowledge.

Table 3 IC address byte

| IC ADDRESS | | | | | | MODE |
|------------|---|---|---|---|---|--------------------|
| 1 | 1 | 0 | 0 | 0 | 0 | 0/1 ⁽¹⁾ |
| | | | | | | R/W ⁽²⁾ |

Notes

1. Defined by address pin FREF:
 - a) 1 = 1st IC address
 - b) 0 = 2nd IC address.
2. Read or write mode:
 - a) 0 = write operation to TEA6840H
 - b) 1 = read operation from TEA6840H.

12.2.2 WRITE MODE: DATA BYTE 1

Table 4 Format of data byte 1

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| AF | PCA6 | PCA5 | PCA4 | PCA3 | PCA2 | PCA1 | PCA0 |

Table 5 Description of data byte 1 bits

| BIT | SYMBOL | DESCRIPTION |
|--------|----------|---|
| 7 | AF | Alternative frequency. If AF = 0, then normal operation. If AF = 1, then AF (RDS) update mode. |
| 6 to 0 | PCA[6:0] | Setting of programmable counter of synthesizer PLL. Upper byte of PLL divider word. |

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12.2.3 WRITE MODE: DATA BYTE 2

Table 6 Format of data byte 2

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PCB7 | PCB6 | PCB5 | PCB4 | PCB3 | PCB2 | PCB1 | PCB0 |

Table 7 Description of data byte 2 bits

| BIT | SYMBOL | DESCRIPTION |
|--------|----------|--|
| 7 to 0 | PCB[7:0] | Setting of programmable counter of synthesizer PLL. Lower byte of PLL divider word. |

12.2.4 WRITE MODE: DATA BYTE 3

Table 8 Format of data byte 3

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| MUTE | DAA6 | DAA5 | DAA4 | DAA3 | DAA2 | DAA1 | DAA0 |

Table 9 Description of data byte 3 bits

| BIT | SYMBOL | DESCRIPTION |
|--------|----------|--|
| 7 | MUTE | FM audio mute. If MUTE = 0, then FM audio not muted. If MUTE = 1, then FM audio muted; writing to programmable divider enabled. |
| 6 to 0 | DAA[6:0] | Setting of antenna digital auto alignment. |

12.2.5 WRITE MODE: DATA BYTE 4

Table 10 Format of data byte 4

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IFMT | RFS2 | RFS1 | RFS0 | IFPR | BND1 | BND0 | AMFM |

Table 11 Description of data byte 4 bits

| BIT | SYMBOL | DESCRIPTION |
|---------|----------|--|
| 7 | IFMT | IF measuring time. If IFMT = 0, then IF measuring time is 20 ms. If IFMT = 1, then IF measuring time is 2 ms. |
| 6 to 4 | RFS[2:0] | Reference frequency for synthesizer. These 3 bits determine the reference frequency, see Table 12. |
| 3 | IFPR | IF counter prescaler ratio. If IFPR = 0, then IF prescaler ratio is 100. If IFPR = 1, then IF prescaler ratio is 10. |
| 2 and 1 | BND[1:0] | Band switch. These 2 bits select in FM mode band and local or distant, see Table 13; in AM mode band and AM stereo, see Table 14. |
| 0 | AMFM | AM or FM switch. If AMFM = 0, then FM mode. If AMFM = 1, then AM mode |

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Table 12 Reference frequency setting

| RFS2 | RFS1 | RFS0 | f _{ref} (kHz) |
|------|------|------|------------------------|
| 0 | 0 | 0 | 100 |
| 1 | 0 | 0 | 50 |
| 0 | 1 | 0 | 25 |
| 1 | 1 | 0 | 20 |
| 0 | 0 | 1 | 10 |
| 1 | 0 | 1 | 10 |
| 0 | 1 | 1 | 10 |
| 1 | 1 | 1 | 10 |

Table 13 FM mode

| BND1 | BND0 | SELECTION |
|------|------|--|
| 0 | 0 | FM standard: dead zone high current charge pump active, FM AGC defined by RF level and threshold level setting by I ² C-bus |
| 0 | 1 | FM local: dead zone high current charge pump active, FM AGC source current set to maximum |
| 1 | 0 | FM East Europe: dead zone high current charge pump switched off, current of low current charge pump set to 1 mA |
| 1 | 1 | FM weather band: N1 divider set to 1 and I and Q phase shift network switched on, WX flag signal activated |

Table 14 AM mode; note 1

| BND1 | BND0 | SELECTION |
|------|------|--|
| 0 | 0 | AM mono; N2 divider set to 5 (SW) |
| 0 | 1 | AM stereo; N2 divider set to 5 (SW) |
| 1 | 0 | AM mono; N2 divider set to 10 (LW, MW) |
| 1 | 1 | AM stereo; N2 divider set to 10 (LW, MW) |

Note

1. In AM mode dead zone high current charge pump switched off, current of low current charge pump set to 1 mA.

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12.2.6 WRITE MODE: DATA BYTE 5

Table 15 Format of data byte 5

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| KAGC | WBA1 | WBA0 | AMSM | TMS3 | TMS2 | TMS1 | TMS0 |

Table 16 Description of data byte 5 bits

| BIT | SYMBOL | DESCRIPTION |
|---------|----------|--|
| 7 | KAGC | Keyed FM AGC. If KAGC = 0, then keyed FM AGC is off. If KAGC = 1, then keyed FM AGC is on. |
| 6 and 5 | WBA[1:0] | Wide band AGC. These 2 bits set the start value of wide band AGC. For AM, see Table 17 and for FM, see Table 18. |
| 4 | AMSM | AM soft mute. If AMSM = 0, then AM soft mute is off. If AMSM = 1, then AM soft mute is on. |
| 3 | TMS3 | In test mode charge pump 3-state. If TMS3 = 0, then 3-state off. If TMS3 = 1, then 3-state on. |
| 2 | TMS2 | In test mode external clock for level and antenna DAA. If TMS2 = 0, then external clock disabled. If TMS2 = 1, then external clock enabled. |
| 1 and 0 | TMS[1:0] | In test mode setting of pin FREF. These 2 bits define the function of pin FREF, see Table 19. |

Table 17 Setting of wide band AGC for AM

| WBA1 | WBA0 | AM MIXER 1 INPUT VOLTAGE (PEAK VALUE) (mV) |
|------|------|---|
| 0 | 0 | 375 |
| 0 | 1 | 500 |
| 1 | 0 | 625 |
| 1 | 1 | 750 |

Table 18 Setting of wide band AGC for FM

| WBA1 | WBA0 | FM RF MIXER INPUT VOLTAGE (RMS VALUE) (mV) |
|------|------|---|
| 1 | 1 | 4 |
| 1 | 0 | 8 |
| 0 | 1 | 12 |
| 0 | 0 | 16 |

Table 19 Setting function of pin FREF in test mode

| TMS1 | TMS0 | OUTPUT AT PIN FREF |
|------|------|--|
| 0 | 0 | reference frequency of TEA688x or TEF689x |
| 0 | 1 | tuner oscillator frequency divided by division ratio of programmable divider |
| 1 | 0 | PLL synthesizer reference frequency |
| 1 | 1 | not used (no output) |

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12.2.7 WRITE MODE: DATA BYTE 6

Table 20 Format of data byte 6

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| LST4 | LST3 | LST2 | LST1 | LST0 | LSL2 | LSL1 | LSL0 |

Table 21 Description of data byte 6 bits

| BIT | SYMBOL | DESCRIPTION |
|--------|----------|---|
| 7 to 3 | LST[4:0] | Setting of level DAA starting point. These 5 bits determine the offset of the level detector output voltage. |
| 2 to 0 | LSL[2:0] | Setting of level DAA slope. These 3 bits determine the steepness of the level detector output voltage. |

Table 22 Standard setting of data byte 6 bits

| SETTING OF LEVEL DAA STARTING POINT | | | | | SETTING OF LEVEL DAA SLOPE | | |
|-------------------------------------|------|------|------|------|----------------------------|------|------|
| LST4 | LST3 | LST2 | LST1 | LST0 | LSL2 | LSL1 | LSL0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

12.2.8 READ MODE: DATA BYTE 1

Table 23 Format of 1st data byte

| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IFC7 | IFC6 | IFC5 | IFC4 | IFC3 | IFC2 | IFC1 | IFC0 |

Table 24 Description of data byte 1 bits

| BIT | SYMBOL | DESCRIPTION |
|--------|----------|--|
| 7 to 0 | IFC[7:0] | IF counter result. These bits contain the last eight bits of the IF counter result. |

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13 TEST AND APPLICATION INFORMATION

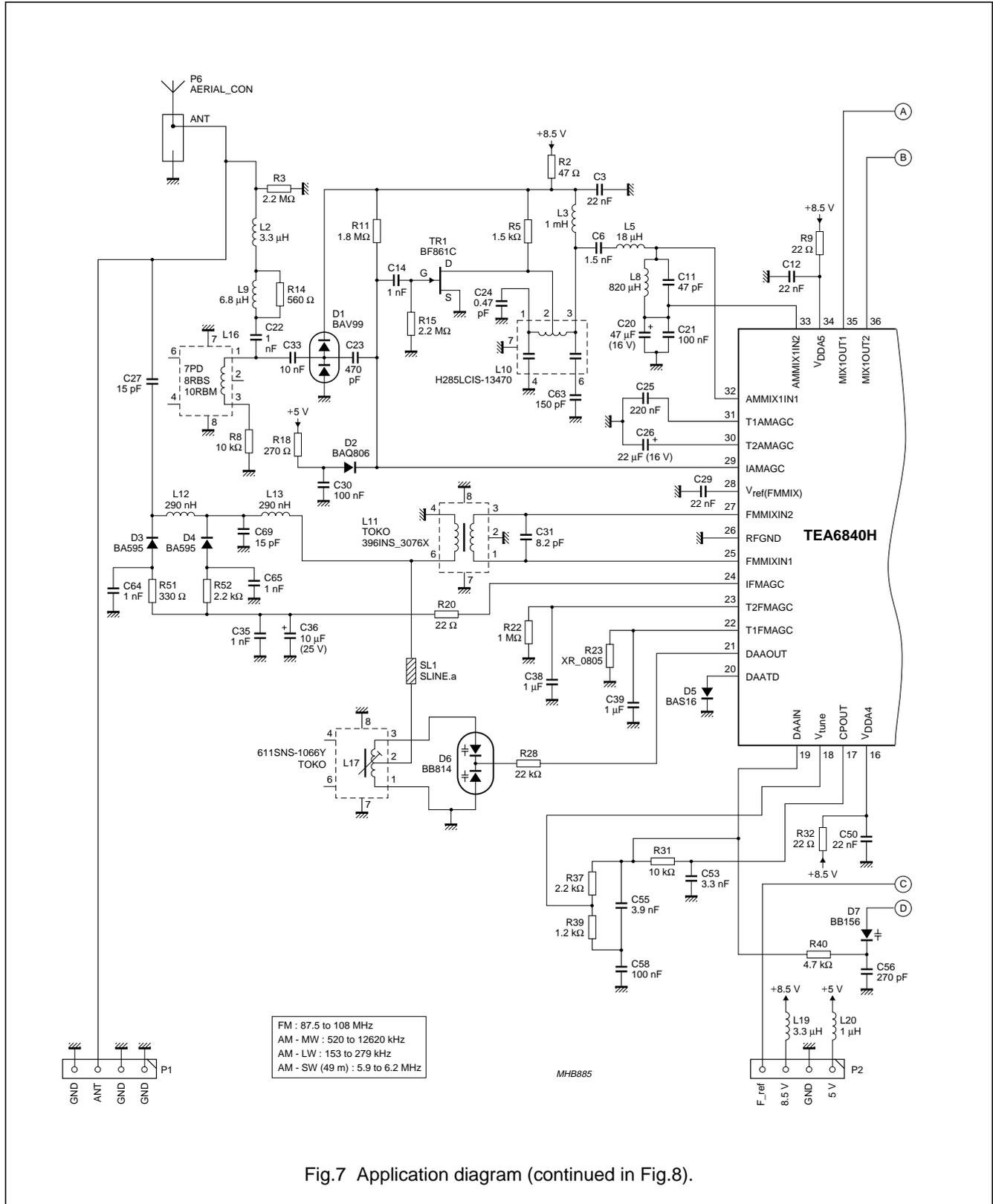


Fig.7 Application diagram (continued in Fig.8).

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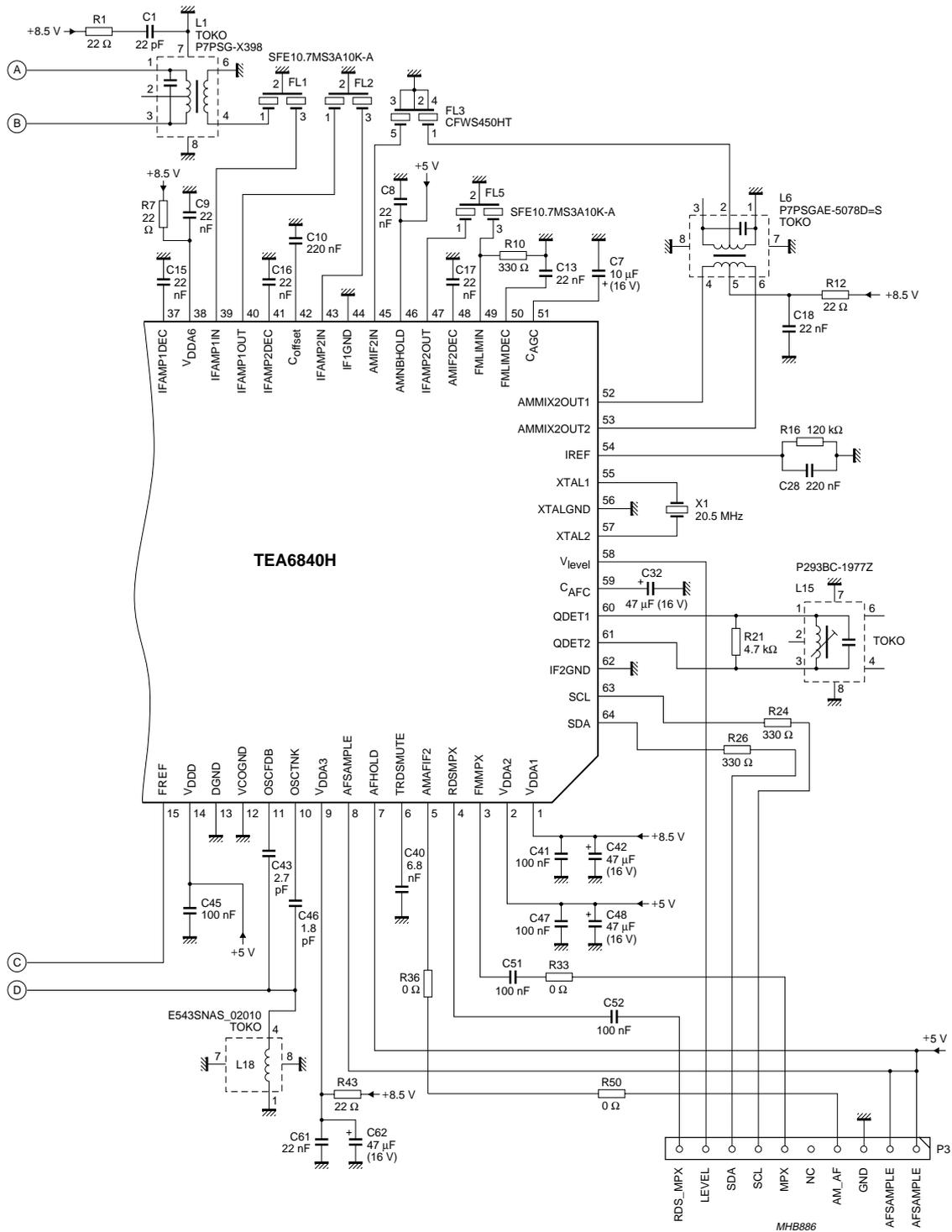


Fig.8 Application diagram (continued from Fig.7).

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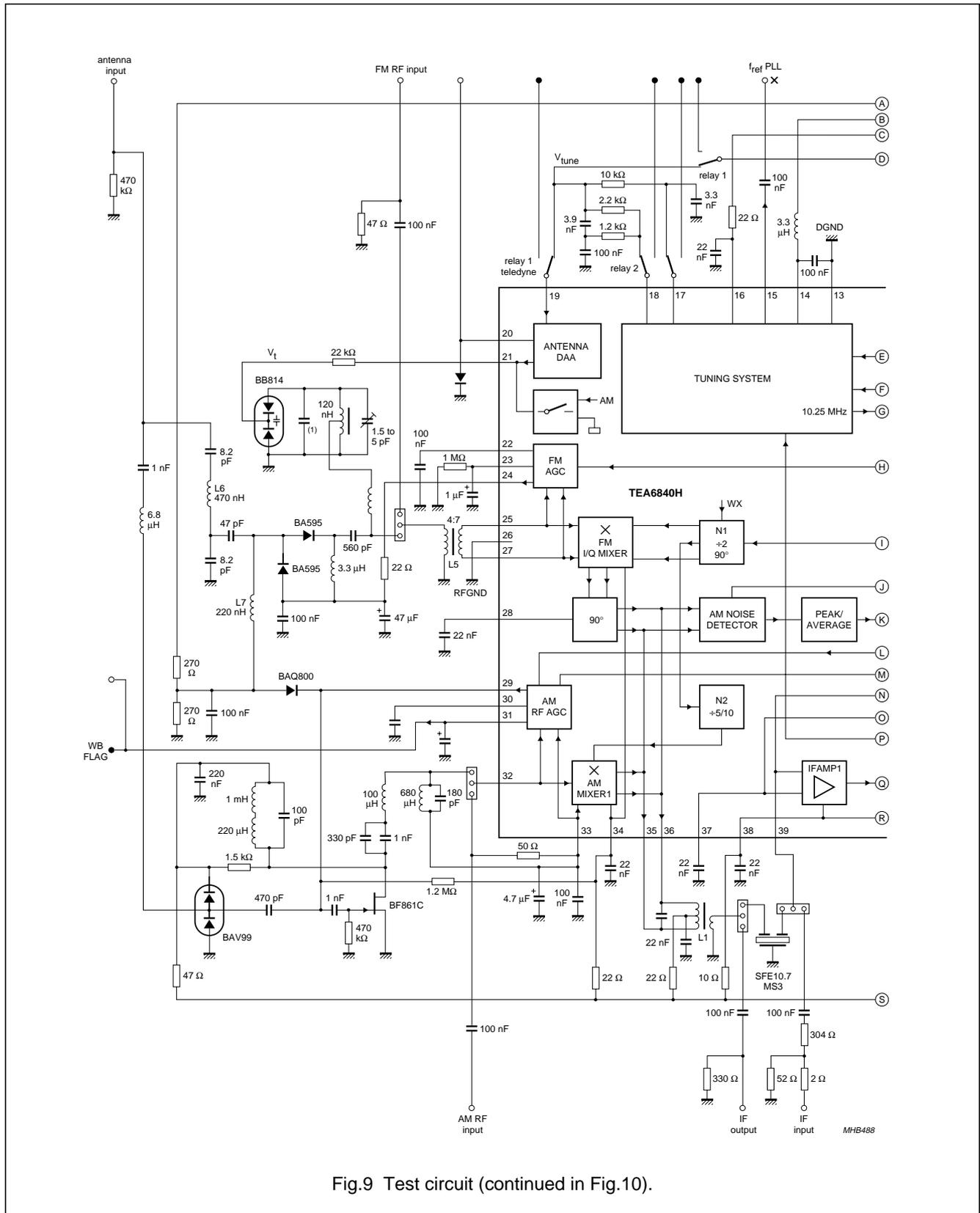
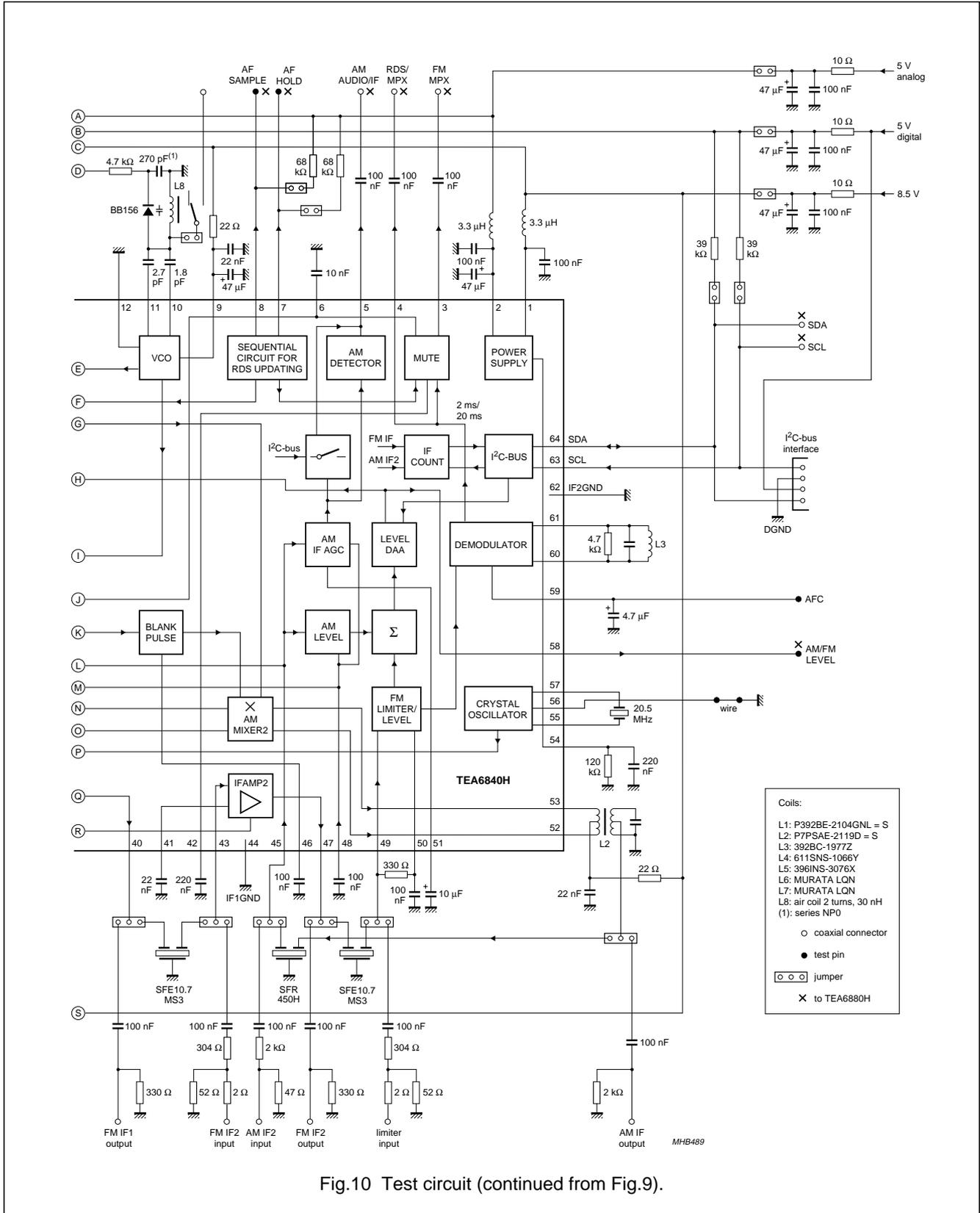


Fig.9 Test circuit (continued in Fig.10).

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Table 25 DC operating points

| SYMBOL | PIN | UNLOADED DC VOLTAGE (V) | | | | | |
|-------------------------|-----|-------------------------|------|------|------------------------|-----------------|----------------------|
| | | AM MODE | | | FM MODE | | |
| | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| V _{DDA1} | 1 | external 8.5 | | | external 8.5 | | |
| V _{DDA2} | 2 | external 5 | | | external 5 | | |
| FMMPX | 3 | floating | | | 3 | 3.5 | 4 |
| RDSMPX | 4 | floating | | | 2.6 | 3.1 | 3.3 |
| AMAFIF2 | 5 | 4 | 4.3 | 4.6 | floating | | |
| TRDSMUTE | 6 | 1.9 | 2.2 | 2.5 | 0.7 (muted) | 1.2 (muted) | 1.7 (muted) |
| | | | | | 5.2 (not muted) | 5.7 (not muted) | 6.2 (not muted) |
| AFHOLD | 7 | open-collector | | | open-collector | | |
| AFSAMPLE | 8 | 0 | 0.2 | 0.5 | 0 | 0.2 | 0.5 |
| V _{DDA3} | 9 | external 8.5 | | | external 8.5 | | |
| OSCTNK | 10 | 5 | 6.1 | 7.2 | 5 | 6.1 | 7.2 |
| OSCFDB | 11 | 2.2 | 2.8 | 3.4 | 2.2 | 2.8 | 3.4 |
| VCOGND | 12 | external 0 | | | external 0 | | |
| DGND | 13 | external 0 | | | external 0 | | |
| V _{DDD} | 14 | external 5 | | | external 5 | | |
| FREF | 15 | 3.2 | 3.4 | 3.7 | 3.2 | 3.4 | 3.7 |
| V _{DDA4} | 16 | external 8.5 | | | external 8.5 | | |
| CPOUT | 17 | 0 | – | 8.5 | 0 | – | 8.5 |
| V _{tune} | 18 | 0 | – | 8.5 | 0 | – | 8.5 |
| DAAIN | 19 | 0 | – | 8.5 | 0 | – | 8.5 |
| DAATD | 20 | floating | | | 0.2 | – | 1.5 |
| DAAOUT | 21 | – | 0.2 | 0.3 | 0.2 | – | 8.25 |
| T1FMAGC | 22 | floating | | | 1 | – | 7 |
| T2FMAGC | 23 | 7.5 | 8 | 8.3 | 3.9 | 4.6 | 5.3 |
| IFMAGC | 24 | floating | | | 1.5 (external biasing) | – | 4 (external biasing) |
| FMMIXIN1 | 25 | 1 | 1.3 | 1.6 | 2.3 | 2.8 | 3.3 |
| RFGND | 26 | external 0 | | | external 0 | | |
| FMMIXIN2 | 27 | 1 | 1.3 | 1.6 | 2.3 | 2.8 | 3.3 |
| V _{ref(FMMIX)} | 28 | 2.7 | 3.1 | 3.4 | 6.5 | 7.1 | 7.9 |
| IAMAGC | 29 | open-collector | | | open-collector | | |
| T2AMAGC | 30 | 2.5 | 2.8 | 3.1 | floating | | |
| T1AMAGC | 31 | 0 | 2.8 | 4.6 | 0 (no WX) | 0.3 (no WX) | 0.5 (no WX) |
| AMMIX1IN1 | 32 | 2.3 | 2.75 | 3.1 | floating | | |
| AMMIX1IN2 | 33 | 2.3 | 2.75 | 3.1 | floating | | |
| V _{DDA5} | 34 | external 8.5 | | | external 8.5 | | |
| MIX1OUT1 | 35 | external 8.5 | | | external 8.5 | | |

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| SYMBOL | PIN | UNLOADED DC VOLTAGE (V) | | | | | |
|---------------------|-----|-------------------------|------|------|--------------|------|------|
| | | AM MODE | | | FM MODE | | |
| | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| MIX1OUT2 | 36 | external 8.5 | | | external 8.5 | | |
| IFAMP1DEC | 37 | 2.4 | 2.7 | 3 | 2.3 | 2.7 | 3.1 |
| V _{DDA6} | 38 | external 8.5 | | | external 8.5 | | |
| IFAMP1IN | 39 | 2.4 | 2.7 | 3 | 2.3 | 2.7 | 3.1 |
| IFAMP1OUT | 40 | 7.2 | 7.9 | – | 3.6 | 4 | 4.4 |
| IFAMP2DEC | 41 | 3 | 4 | 5 | 2.7 | 3.1 | 3.5 |
| C _{offset} | 42 | floating | | | 3 | 3.5 | 4 |
| IFAMP2IN | 43 | 3 | 4 | 5 | 2.7 | 3.1 | 3.5 |
| IF1GND | 44 | external 0 | | | external 0 | | |
| AMIF2IN | 45 | 2.4 | 2.7 | 3.2 | floating | | |
| AMNBHOLD | 46 | 4.3 | 4.6 | 5.1 | 8 | 8.4 | – |
| IFAMP2OUT | 47 | 7.2 | 7.9 | – | 3.4 | 3.9 | 4.4 |
| AMIF2DEC | 48 | 2.4 | 2.7 | 3.2 | floating | | |
| FMLIMIN | 49 | 2.5 | 3 | 3.5 | 2.5 | 2.8 | 3.1 |
| FMLIMDEC | 50 | 2.5 | 3 | 3.5 | 2.5 | 2.8 | 3.1 |
| C _{AGC} | 51 | 3.6 | 4.3 | 4.8 | 4.1 | 4.6 | 5.1 |
| AMMIX2OUT1 | 52 | external 8.5 | | | external 8.5 | | |
| AMMIX2OUT2 | 53 | external 8.5 | | | external 8.5 | | |
| IREF | 54 | 4 | 4.25 | 4.5 | 4 | 4.25 | 4.5 |
| XTAL1 | 55 | 1.7 | 2.1 | 2.5 | 1.7 | 2.1 | 2.5 |
| XTALGND | 56 | external 0 | | | external 0 | | |
| XTAL2 | 57 | 1.7 | 2.1 | 2.5 | 1.7 | 2.1 | 2.5 |
| V _{level} | 58 | 0.05 | – | 7 | 0 | – | 7 |
| C _{AFC} | 59 | floating | | | 1.2 | 3.4 | 4.1 |
| QDET1 | 60 | floating | | | 3.6 | 4.1 | 4.6 |
| QDET2 | 61 | floating | | | 3.6 | 4.1 | 4.6 |
| IF2GND | 62 | external 0 | | | external 0 | | |
| SCL | 63 | 4.8 | 5 | 5.2 | 4.8 | 5 | 5.2 |
| SDA | 64 | 4.8 | 5 | 5.2 | 4.8 | 5 | 5.2 |

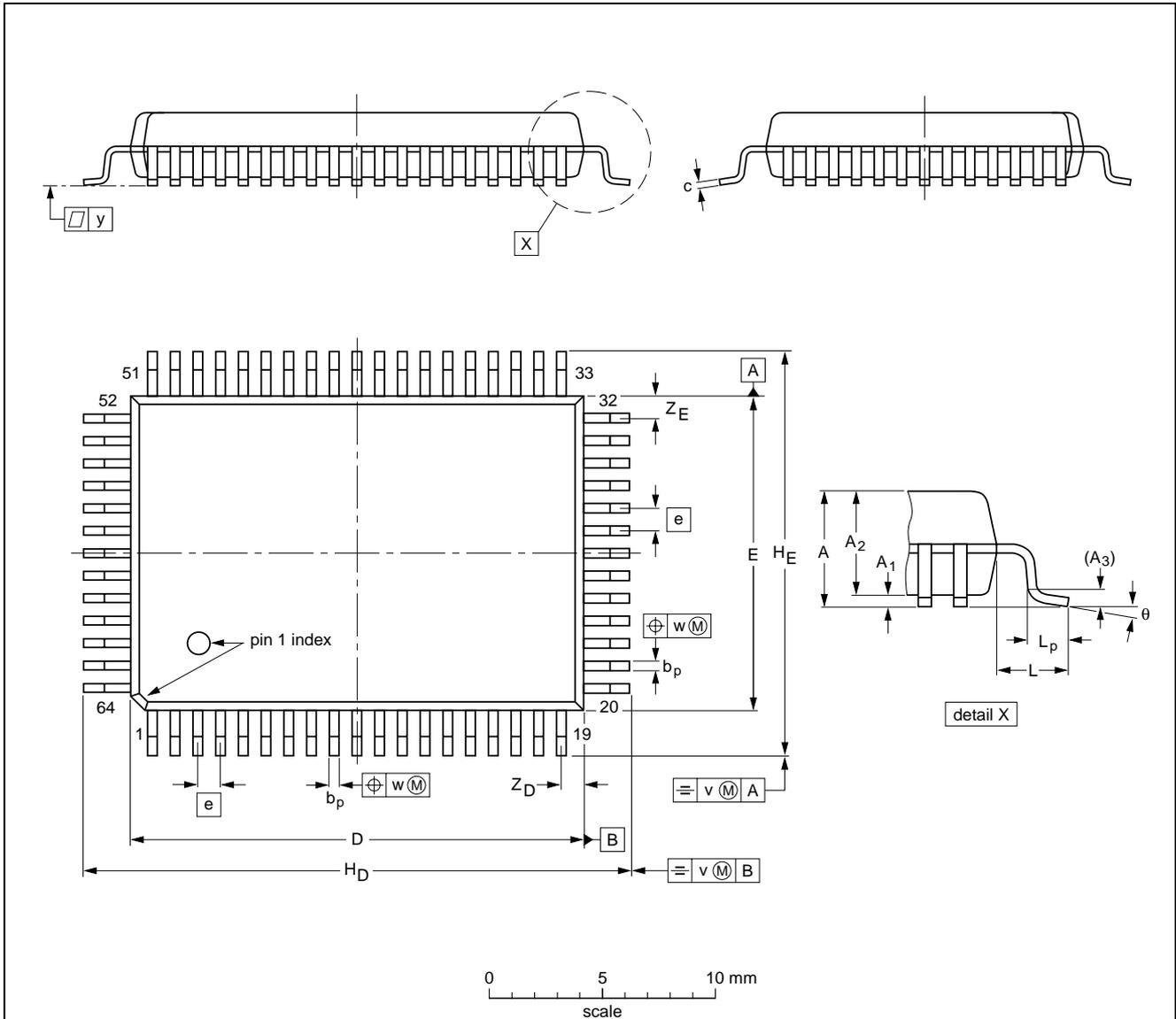
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14 PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT319-2



DIMENSIONS (mm are the original dimensions)

| UNIT | A _{max.} | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _D | H _E | L | L _p | v | w | y | Z _D ⁽¹⁾ | Z _E ⁽¹⁾ | θ |
|------|-------------------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|---|----------------|----------------|------|----------------|-----|-----|-----|-------------------------------|-------------------------------|----------|
| mm | 3.20 | 0.25 0.05 | 2.90 2.65 | 0.25 | 0.50 0.35 | 0.25 0.14 | 20.1 19.9 | 14.1 13.9 | 1 | 24.2 23.6 | 18.2 17.6 | 1.95 | 1.0 0.6 | 0.2 | 0.2 | 0.1 | 1.2 0.8 | 1.2 0.8 | 7° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT319-2 | | MO-112 | | | | 97-08-01 99-12-27 |

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15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE ⁽¹⁾ | SOLDERING METHOD | |
|--|-----------------------------------|-----------------------|
| | WAVE | REFLOW ⁽²⁾ |
| BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA | not suitable | suitable |
| DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS | not suitable ⁽³⁾ | suitable |
| PLCC ⁽⁴⁾ , SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended ⁽⁴⁾⁽⁵⁾ | suitable |
| SSOP, TSSOP, VSO | not recommended ⁽⁶⁾ | suitable |

Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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16 DATA SHEET STATUS

| LEVEL | DATA SHEET STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾⁽³⁾ | DEFINITION |
|-------|----------------------------------|----------------------------------|--|
| I | Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| II | Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| III | Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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TEA6840H**19 PURCHASE OF PHILIPS I²C COMPONENTS**

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Printed in The Netherlands

753503/03/pp48

Date of release: 2003 Feb 04

Document order number: 9397 750 10543

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